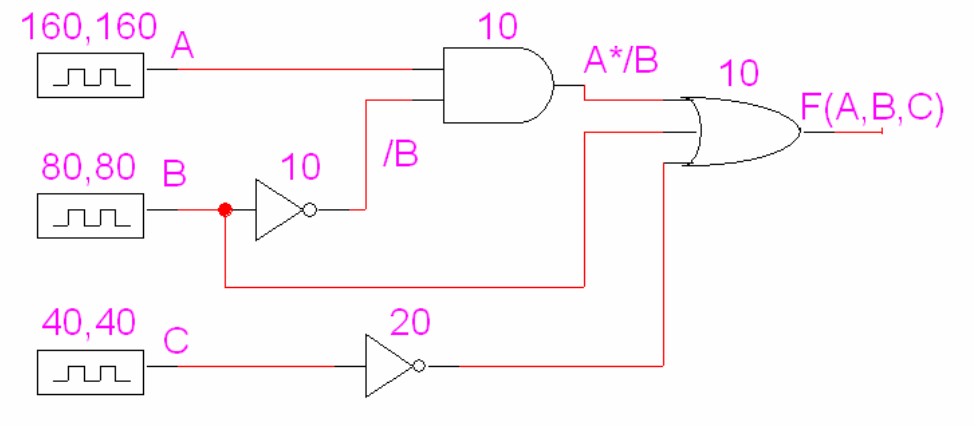
Name _____ CM _____ Due date: Tuesday, Sept. 16

ECE130-03 Homework #4 (LogicWorks 4) Fall 2003

1 Simulate the following circuit with LogicWorks 4 for the two cases in (a) and (b). Submit snapshots of your circuit schematics and annotated waveforms.



(a) Print waveforms of A, B, C and F(A,B,C) with zero time delay gates for one period of A and reference lines of 10-unit-time intervals. Annotate the waveforms to show F(A,B,C). Fill in the truth table for F(A,B,C) below.

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(b) Print waveform of A, B, C and F(A,B,C) with gate delays as shown in the above schematic for one period of signal A and reference lines of 10 time unit intervals. Make sure to reset your simulation and avoid the first period, which may not show the delay effect.

(c) What observation can you make on the output waveform of F(A,B,C) in Part (b)?