Name _____ CM _____ Due date: Monday, Nov. 3

ECE130-03 **Homework #21** **Fall 2003**

(Controller design)

1 4-bit multiplication can be done by a series of 1-bit SHIFT and 4-bit ADD operations. For example, 0101 X 1001 can be done as follows. Assume multiplicand A=0101, multiplier B=1001 and partial sum S(7:4)S(3:0)= 00000000. Starting from the least significant bit B0 of the multiplier B, if B0=1 then add the multiplicand A to the upper nibble S(7:4) of the partial sum and if B0=0, add zero to S(7:4). Shift the partial sum S(7:4)S(3:0 to the right with carry. Repeat for B1, B2, B3 and then stop. Here are the steps in detail.

Step 0: Clear S(7:4)S(3:0) =00000000.
Step 1: B0=1, S(7:4) = 0000+0101= 0101
Step 2: Right one bit shift S(7:4) and S(3:0) with carry to obtain S(7:4)S(3:0)=00101000
Step 3: B1=0, S(7:4) = 0010+0000=0010
Step 4: Right shift one bit S(7:4) and S(3:0) with carry to obtain S(7:4)S(3:0)=00010100
Step 5: B2=0, S(7:4) = 0001+0000=0001
Step 6: Right shift one bit S(7:4) and S(3:0) with carry to obtain S(7:4)S(3:0)=00001010
Step 7: B3=1, S(7:4) = 0000+0101=0101
Step 8: Right shift one bit S(7:4) and S(3:0) with carry to obtain S(7:4)S(3:0)=00101101

```
   0101
X  1001
------
   0101
  0000
 0000
0101
-------
0101101
```

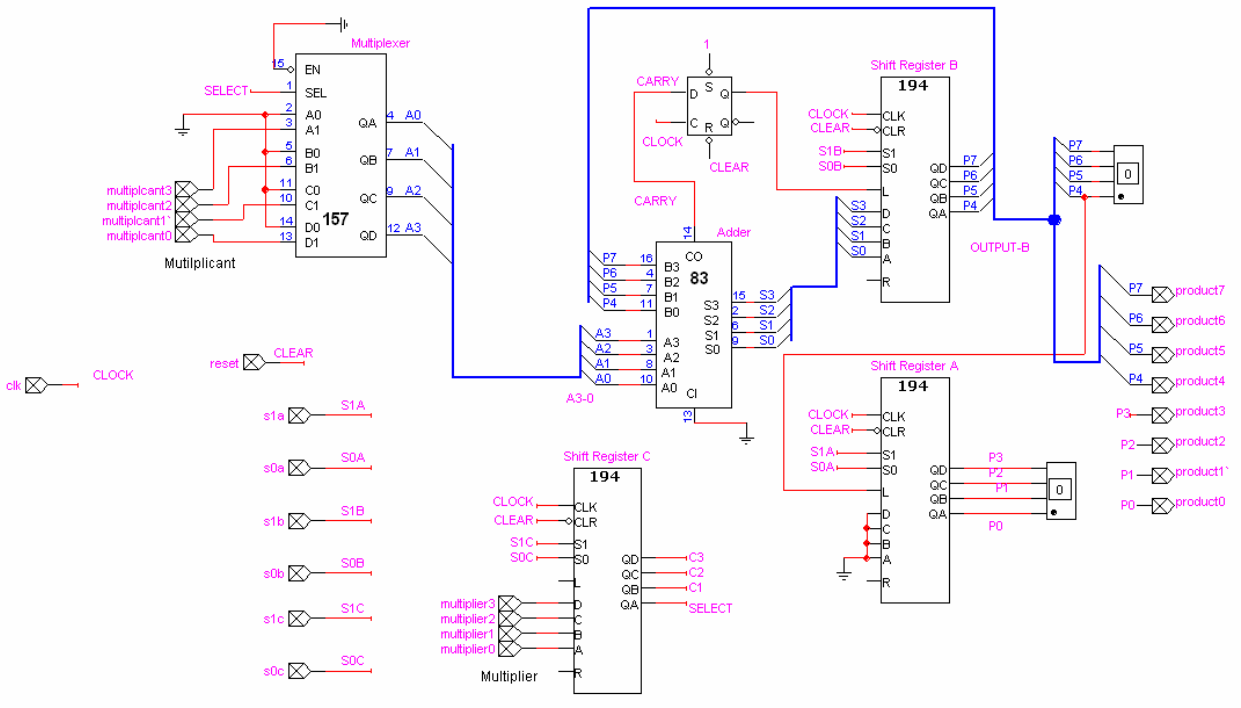
The circuit on next page is the data unit device test and subcircuit of a multiplier by shift-and-add. The LogicWorks file of the device test circuit is in **G:\ee\yoder\ece130\Homework**.

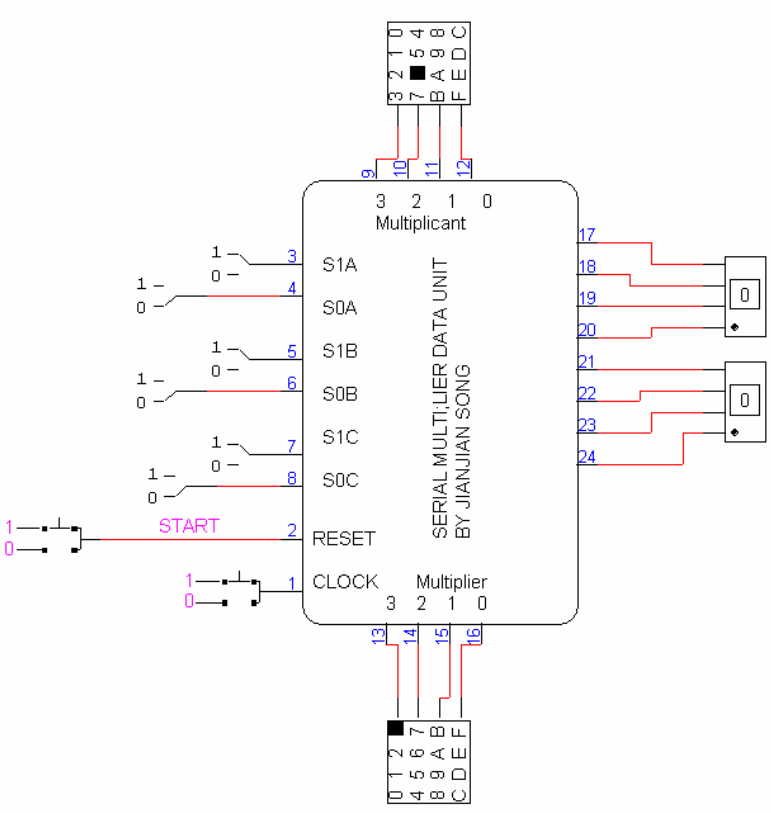
Registers and their modes of operation are as follows.

	Reset to start	Clock cycle									
Register	0	1	2	3	4	5	6	7	8	9	10
A (high byte)	Reset	Hold	Hold	LS	Hold	LS	Hold	LS	Hold	LS	Hold
B (lower byte)	Reset	Hold	Load	LS	Load	LS	Load	LS	Load	LS	Hold
C (multiplier)	Reset	Load	Hold	LS	Hold	LS	Hold	LS	Hold	LS	Hold

Design a controller for this data unit so that the output will show two digit product each time a push button is pressed to start the multiplication sequence. Implement your controller with a counter and a ROM. The ROM outputs a sequence of ten control signals for S1A, S0A, S2B, S0B, S1C and S0C. The counter drives the address pins of the ROM.

Replace the binary switch on the clock wire with a clock generator. After the START button is pressed and released, the counter should generate a sequence of addresses to send control signals at the output to the ROM to the data unit. The counter should hold the address line after the ten clock cycles. Email your solution to Mark.A.Yoder@Rose-Hulman.edu by the due date. Use the subject: **ece130: HW21**.


Multiplexer
SELECT
multiplcant3
multiplcant2
multiplcant1
multiplcant0
Mutilplicant
157
CARRY
CLOCK
CLEAR
Shift Register B
194
Adder
83
OUTPUT-B
Shift Register A
Shift Register C
Multiplier
reset
clk
s1a
s0a
s1b
s0b
s1c
s0c
A3-0
product7
product6
product5
product4
product3
product2
product1
product0


Multiplicant
S1A
S0A
S1B
S0B
S1C
S0C
START
RESET
CLOCK
Multiplier
SERIAL MULTI;LIER DATA UNIT
BY JIANJIAN SONG