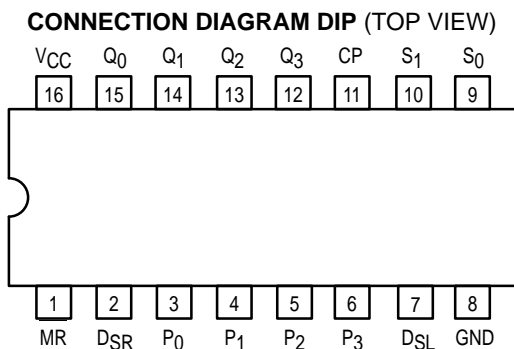




# 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The SN54/74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL families.

- Typical Shift Frequency of 36 MHz
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects



### PIN NAMES

S <sub>0</sub> , S <sub>1</sub>	Mode Control Inputs
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs
DSR	Serial (Shift Right) Data Input
DSL	Serial (Shift Left) Data Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q <sub>0</sub> -Q <sub>3</sub>	Parallel Outputs (Note b)

### LOADING (Note a)

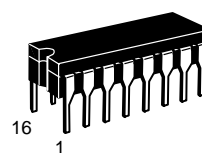
	HIGH	LOW
S <sub>0</sub> , S <sub>1</sub>	0.5 U.L.	0.25 U.L.
P <sub>0</sub> -P <sub>3</sub>	0.5 U.L.	0.25 U.L.
DSR	0.5 U.L.	0.25 U.L.
DSL	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q <sub>0</sub> -Q <sub>3</sub>	10 U.L.	5 (2.5) U.L.

### NOTES:

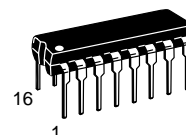
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.  
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

## SN54/74LS194A

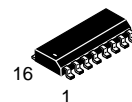
### 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08



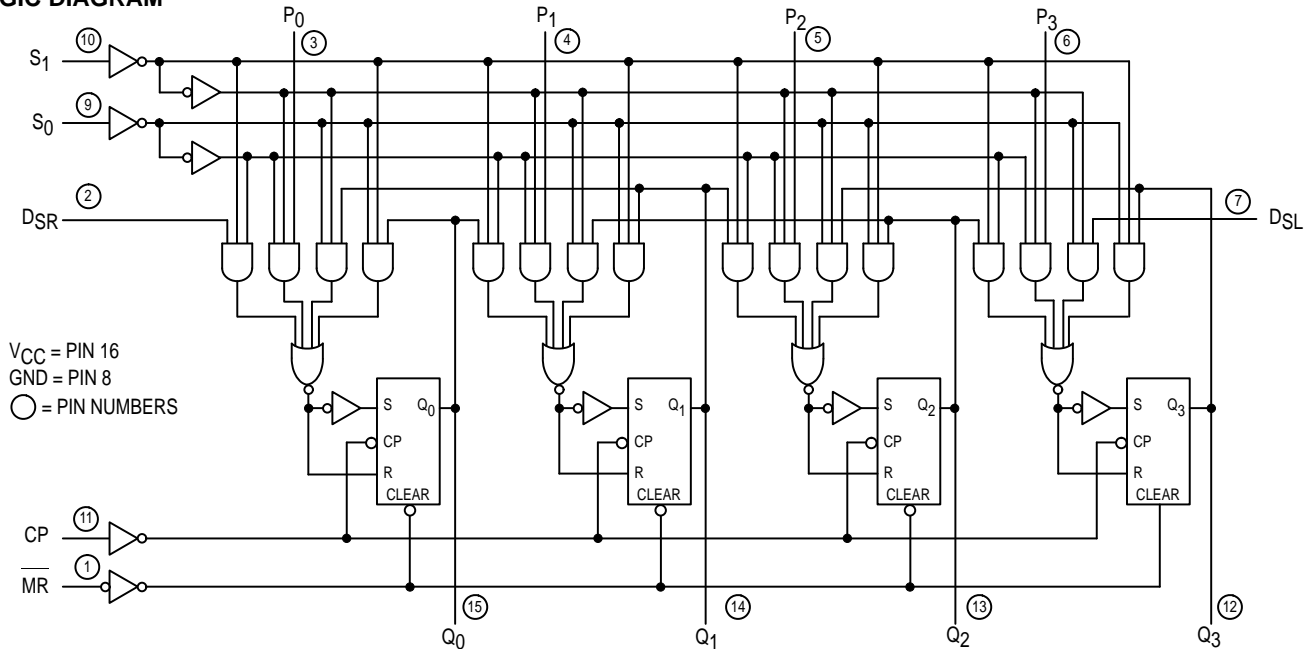
**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

# SN54/74LS194A

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the Motorola LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

The four parallel data inputs ( $P_0$ ,  $P_1$ ,  $P_2$ ,  $P_3$ ) are D-type inputs. When both  $S_0$  and  $S_1$  are HIGH, the data appearing on  $P_0$ ,  $P_1$ ,  $P_2$ , and  $P_3$  inputs is transferred to the  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and

$Q_3$  outputs respectively following the next LOW to HIGH transition of the clock.

The asynchronous Master Reset ( $\overline{MR}$ ), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

Two mode control inputs ( $S_0$ ,  $S_1$ ) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right,  $Q_0 \rightarrow Q_1$ , etc.) or right to left (shift left,  $Q_3 \rightarrow Q_2$ , etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both  $S_0$  and  $S_1$  are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

D-type serial data inputs ( $DSR$ ,  $DSL$ ) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

## MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	MR	$S_1$	$S_0$	$DSR$	$DSL$	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	$q_0$	$q_1$	$q_2$	$q_3$
Shift Left	H	h	l	X	l	X	$q_1$	$q_2$	$q_3$	L
	H	h	l	X	h	X	$q_1$	$q_2$	$q_3$	H
Shift Right	H	l	h	l	X	X	L	$q_0$	$q_1$	$q_2$
	H	l	h	h	X	X	H	$q_0$	$q_1$	$q_2$
Parallel Load	H	h	h	X	X	$P_n$	$P_0$	$P_1$	$P_2$	$P_3$

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition

$p_n$  ( $q_n$ ) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

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## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			23	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	25	36		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		14 17	22 26	ns	
t <sub>PHL</sub>	Propagation Delay, MR to Output		19	30	ns	

# SN54/74LS194A

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock or MR Pulse Width	20			ns	$V_{CC} = 5.0\text{ V}$
$t_S$	Mode Control Setup Time	30			ns	
$t_S$	Data Setup Time	20			ns	
$t_H$	Hold time, Any Input	0			ns	
$t_{rec}$	Recovery Time	25			ns	

## DEFINITIONS OF TERMS

**SETUP TIME ( $t_S$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

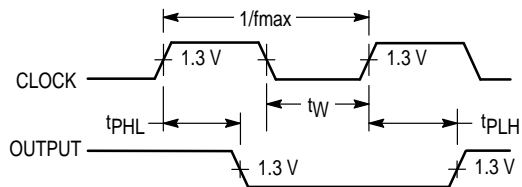
**HOLD TIME ( $t_H$ )** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

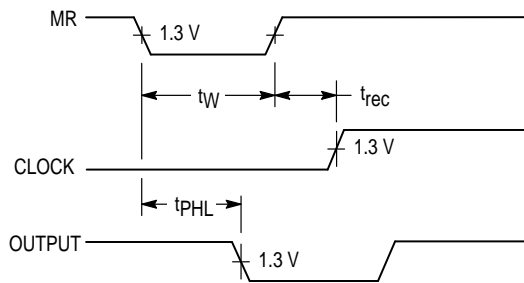
## AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



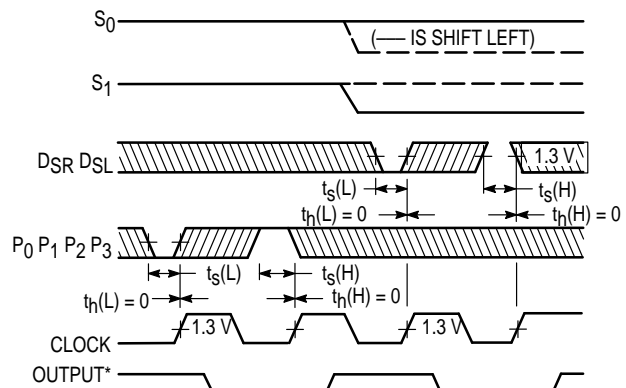
OTHER CONDITIONS:  $S_1 = L, \overline{MR} = H, S_0 = H$

**Figure 1. Clock to Output Delays Clock Pulse Width and  $f_{max}$**



OTHER CONDITIONS:  $S_0, S_1 = H$   
 $P_0 = P_1 = P_2 = P_3 = H$

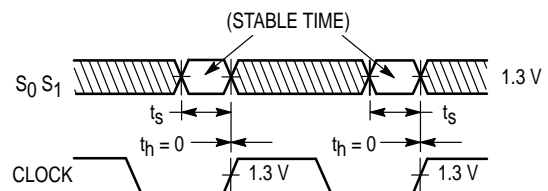
**Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



OTHER CONDITIONS:  $\overline{MR} = H$

\* $D_{SR}$  SET-UP TIME AFFECTS  $Q_0$  ONLY  
 $D_{SL}$  SET-UP TIME AFFECTS  $Q_3$  ONLY

**Figure 3. Setup ( $t_S$ ) and Hold ( $t_H$ ) Time for Serial Data ( $D_{SR}, D_{SL}$ ) and Parallel Data ( $P_0, P_1, P_2, P_3$ )**



OTHER CONDITIONS:  $\overline{MR} = H$

**Figure 4. Setup ( $t_S$ ) and Hold ( $t_H$ ) Time for S Input**