Name _____ CM _____ Due date: Thursday, Oct. 23

ECE130 Homework #18 Fall 2003

(sequential circuit design)

Submit a hard copy of your solution and Be sure to include a printout of your LogicWorks simulator that shows both the circuit diagram and a timing diagram.

1 Derive a Moore state diagram for a sequence detector circuit that has one input X and one output Z. Z is "1" if and only if X has a consecutive sequence of 110 or 010 with the right most bit being the latest. Z is "0" otherwise. The circuit will return to the initial state as soon as one of the two sequences has been detected and will start looking for a new sequence again. Use letters a, b, c, d, etc. to represent states. An example time sequence is given below.

Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
X	1	1	0	0	1	0	0	1	1	1	1	0	0	0	0	1	0	1	1	0
Z	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1

2 (Problem 11 on page 73 of Dr. Eccles' Book) Design a Moore circuit that will produce an output Z=1 if two 0s come together in the input stream X. Z is held to be 1 until a 1 appears at X again. Implement your circuit with one J-K flip-flop and one T-flip-flop. Choose one flip-flop for one bit and the other for another bit in whichever order you want.

Simulate your circuit with LogicWorks. Make sure the two flip-flops are triggered on the same clock edge. Include your schematic and timing diagram from LogicWorks with your solution.

State Diagram:

Present state/input			Next state/output			Flip-flop input values			

