

Name \_\_\_\_\_

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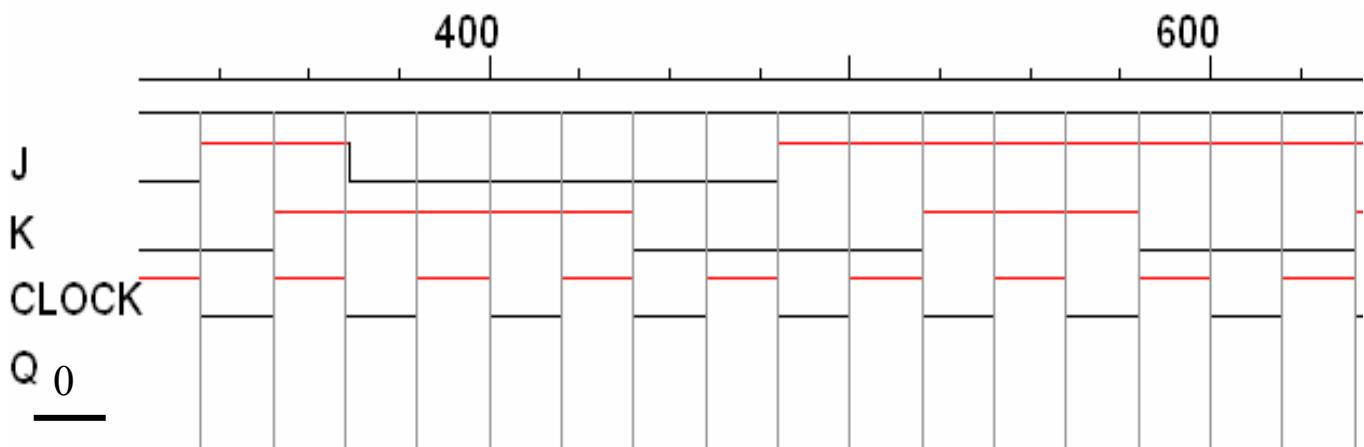
Due date: Monday, Oct. 13

ECE130-03

Homework #14  
(flip-flops)

Fall 2003

- 1 Draw the output waveform Q of a positive-edge triggered J-K flip-flop in the following timing diagram, assuming zero-delay time and Q is at "0" initially. (Note: an input is assumed to have the value before a clock edge if the input changes its value at the clock edge.)



- 2 Draw the output waveform Q of a negative-edged triggered D flip-flop in the following timing diagram, assuming zero-delay time and Q is at "0" initially. (Note: an input is assumed to have the value before a clock edge if the input changes its value at the clock edge.)

