| Name | CM | Due date: Thursday, 2 Oct. 2003 |
|---|---------------------------------|---------------------------------------|
| ECE130-03 | Homework #10 (Multiplexters) | Fall 2003 |
| 1 (Modified Problem 11 on pa Dr. Eccles' book) Implemen Z(A,B,C)=Π(0,2,3,7) using multiplexer. | age 58 of nt an 8-to-1 | A A A A A A A A A A A A A A A A A A A |

2 Fill in K-map for function F(A,B,C,D) that is implemented by a 4-to-1 multiplexer and gates as in the following schematic.



3 (Multiplexer) Implement the 2-bit unsigned-number half subtractor Homework #9 with 74LS151 multiplexer chips and necessary gates. The four inputs are X=X1X0 and Y=Y1Y0. The outputs are two-bit difference D=D1D0 and one-bit borrow B. X1X0 - Y1Y0 = D1D0 B. Borrow occurs when X<Y.

Simulate your design with LogicWorks 4. Submit both your circuit schematic and annotated waveforms with zero gate delay.

| | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 00 | | | | |
| 01 | | | | |
| 11 | | | | |
| 10 | | | | |

| X1X0Y1Y0 | D1 | D0 | Borrow |
|----------|----|----|--------|
| 0000 | | | |
| 0001 | | | |
| 0010 | | | |
| 0011 | | | |
| 0100 | | | |
| 0101 | | | |
| 0110 | | | |
| 0111 | | | |
| 1000 | | | |
| 1001 | | | |
| 1010 | | | |
| 1011 | | | |
| 1100 | | | |
| 1101 | | | |
| 1110 | | | |
| 1111 | | | |