Name _____ CM _____ Due date: Thursday, 25 Sept. 2003

ECE130-03 Homework #7 Fall 2003

(Combinational Circuit Design)

1 Fill the following truth table for a two-bit adder that will generate a two-bit sum S_1 S_0 and one-bit carry C from A_1 A_0 + B_1 B_0,where A_1 A_0 and B_1 B_0 are two bit unsigned numbers.

Obtain a minimized sum-of-products expression for C and a minimized product-of-sums expression for S_0.

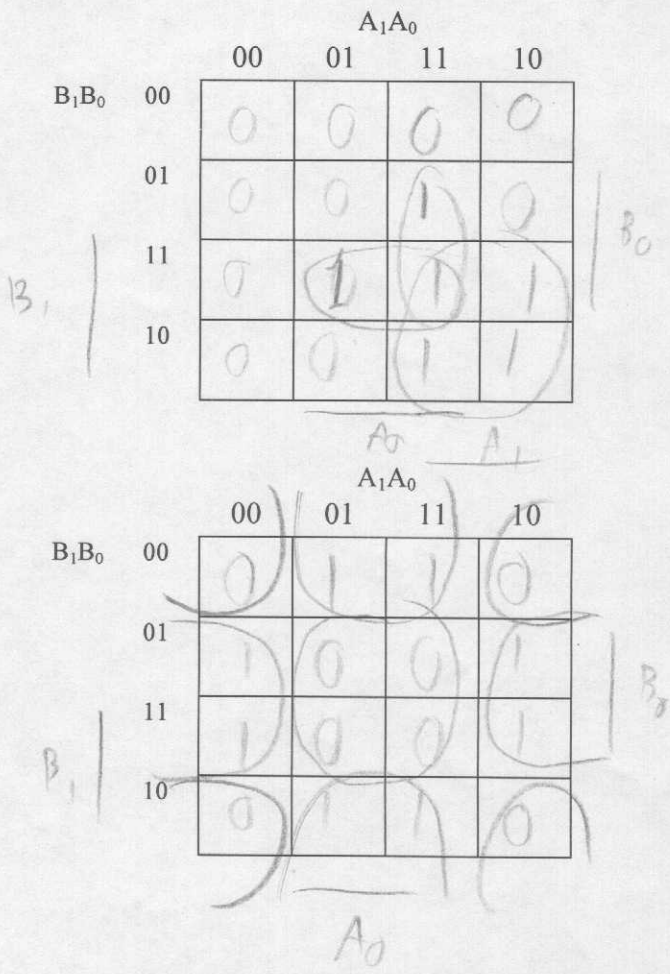
Build an NAND-NAND circuit for C and an NOR-BOR circuit for S_0 with gates from Simulation.Gate.clf library on LogicWorks 4. Set all gate delays to be zero and simulate the circuits to find all possible output combinations. Tie the unused gate inputs to proper logic values.

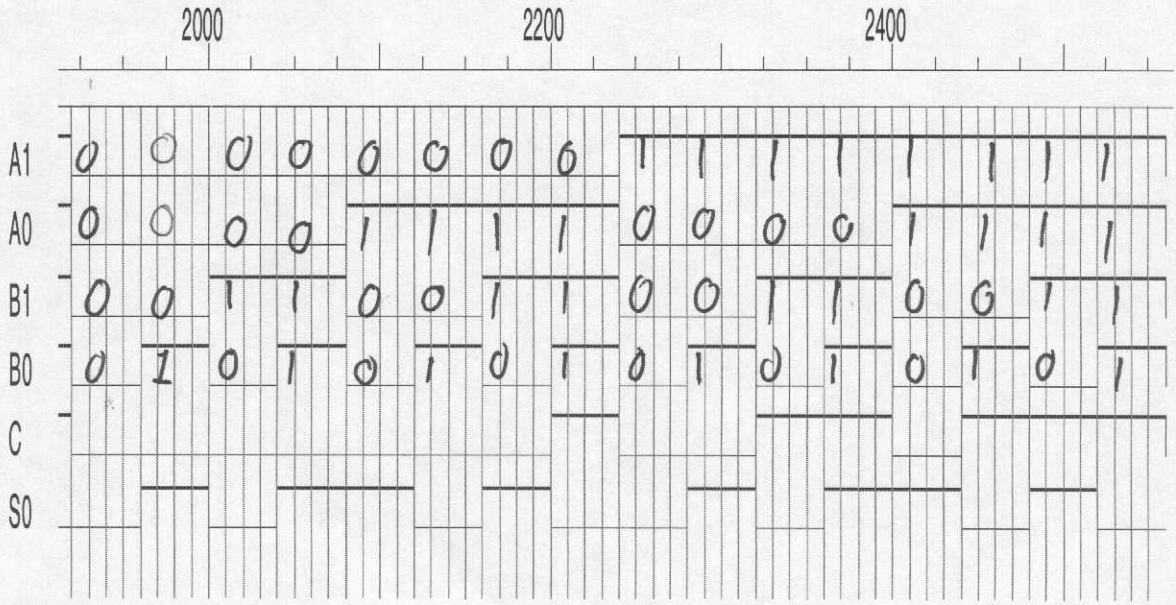
Attach the circuit schematic with all delays visible and one segment of the six waveforms showing all input combinations. Mark the truth table on the waveforms.

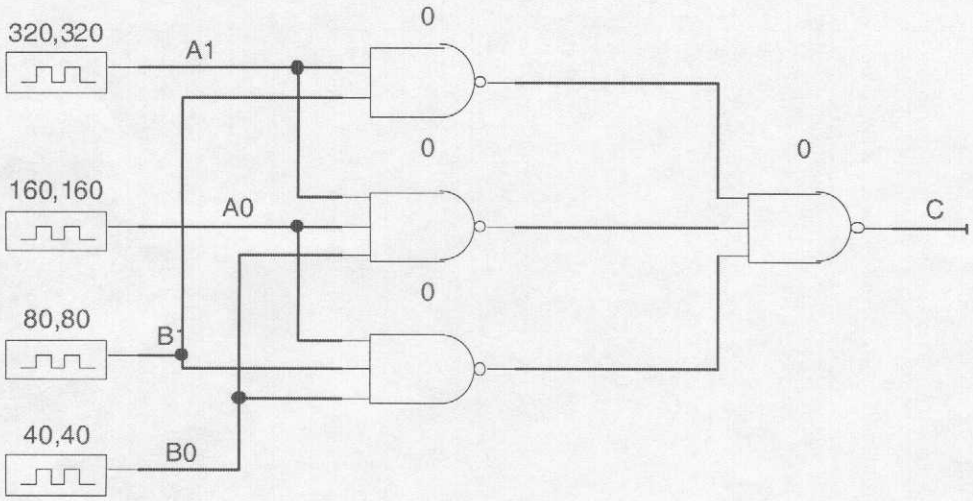
C = $A_1B_1 + A_1A_0B_0 + A_0B_1B_0$

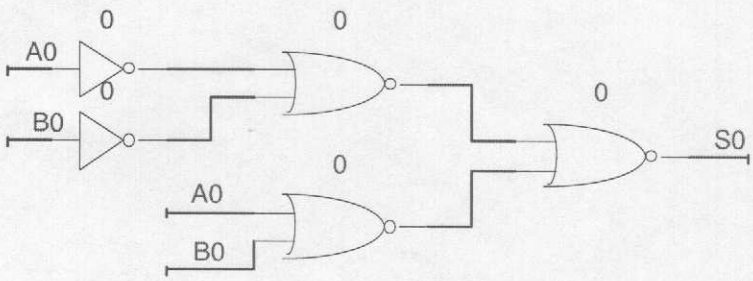
S_0 = $(\bar{A}_0 + \bar{B}_0)(A_0 + B_0)$

A_1	A_0	B_1	B_0	C	S_1	S_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0




2000
2200
2400
A1
A0
B1
B0
C
S0


320,320
A1
160,160
A0
80,80
B1
40,40
B0
0
0
0
0
C


A0
B0
A0
B0
0
0
0
0
0
S0