ECE130-01 Introduction to Logic Design

Fall Quarter 2003

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Textbook: Pragmatic Logic: A Non-idealistic, Practical, Opinionated Look at Digital Logic Design. William J. Eccles (available from the bookstore)

Simulation software: LogicWorks-4 for Windows from Capilano Computing (available from the bookstore)

Course Objectives Fundamental concepts, analysis and design techniques of digital systems will be introduced through examples and simulation. Digital system design processes and methodologies will be discussed and practiced with homework problems and a team project. Upon the completion of this course, the student should be able to analyze and design combinational and sequential circuits as well as to complete a digital system design project from conceptual development, sub-module designs, to system integration.

Grading Policy:

Homework:	10%
In-class exercises & quizzes	5%
Three Tests:	45%
Project:	20%
Final Exam:	20%

Homework: Homework may be assigned daily. Late homework will be accepted with a grade reduction of 20% for each day that it is late.

Tests: The three full-class-period tests and the final exam are closed book and closed notes. The final exam will be scheduled in the exam week.

Project: A team design project will be assigned during the last two weeks. The project description will be distributed later. Grading for the project will have the following breakdowns.

Block Diagram Memo	5%	Simulation	15%
State Diagram Memo	10%	Final Written Report	35%
Verification Memo	15%	Oral Presentation	20%

ECE130-01/03/04 - Introduction to Logic Design

Tentative course Schedule - Fall 2003

Week	Day	Date	Topic	Recommended Reading	tentative homework assignments
0	Thur	4-Sep	Introduction & switching circuits		hw1 assigned
	Fri	5-Sep	logic expression & turn-signal circuit	1.1-1.3	hw1 due/ hw2 assigned
1	Mon	8-Sep	in-class combinational circuit lab	1.1-1.3	hw2 due
	Tue	9-Sep	number systems & 2's complement, binary arithmetic	2	hw3 assigned
	Thur	11-Sep	binary addition and subtraction	2.4	
	Fri	12-Sep	LogicWorks tutorial (bring your laptop)	1.7	hw4 assigned
2	Mon	15-Sep	Boolean algebra, canonical forms	3	hw3, 4 due/ hw5 assigned
	Tue	16-Sep	Boolean algebra, canonical forms	3	
	Thur	18-Sep	Simplification with Kmaps & don't cares		hw5 due/hw6 assigned
	Fri	19-Sep	no class		
3	Mon	22-Sep	Design, NAND-NAND, NOR-NOR	4	hw6 due/hw7 assigned
	Tue	23-Sep	waveforms, delay, Review		hw7 due/hw8 assigned
	Thur	25-Sep	**Test #1**		hw8 due
	Fri	26-Sep	Decoders	5.1	hw9 assigned
4	Mon	29-Sep	Multiplexers	5.2	hw9 due/hw10 assigned
	Tue	30-Sep	HEX, BCD, adder chip, MSI design	2.5, 5.3, 5.6	
	Thur	2-Oct	Hazards, glitches	5.5	hw11 assigned
	Fri	3-Oct	map-entered variables, bus		hw12 assigned
5	Mon	6-Oct	review		hw10, 11, 12 due
	Tue	7-Oct	Introduction to flip-flops	6.1	hw13 assigned
	Thur	9-Oct	**Test #2**		hw13 due
	Fri	10-Oct	Sequential Circuit Analysis: D ff example		hw14, 15 assigned
6	Mon	13-Oct	Sequential Circuit Analysis: JK ff example	6.1, 6.2	hw14, 15 due, hw16
	Tue	14-Oct	LogicWorks Tutorial #2: device symbol		hw16 due, hw17
Fall Break			16-17 October		
7	Mon	20-Oct	Sequence detector design	6.3-6.4	hw17 due
	Tue	21-Oct	railroad crossing	6.3-6.4	hw18
	Thur	23-Oct	Counters	7.1	hw19, hw17 due
	Fri	24-Oct	Shift Registers	7.2	hw20, hw18 due
8	Mon	27-Oct	in-class lab with counter and 7-segment display		hw20, hw18 due
	Tue	28-Oct	pop vending machine, project assigned	8	hw19, 20 due
	Thur	30-Oct	stopwatch controller	8	
	Fri	31-Oct	**Test #3**		group leaders elected
9	Mon	3-Nov	Design Project		
	Tue	4-Nov	Design Project		Block Diagram Memo
	Thur	6-Nov	Design Project		
	Fri	7-Nov	Design Project		State Diagram Memo
10	Mon	10-Nov	Design Project		
	Tue	11-Nov	Design Project		Verification Memo
	Thur	13-Nov	quarter review		**Project Reports Due**
	Fri	14-Nov	Project Presentation		
	Mon	17-Nov	**Final Exam**		To be scheduled