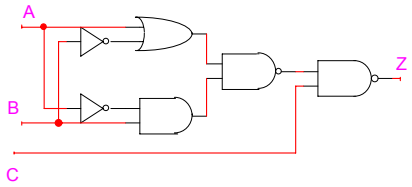
1 (15 points) A logic output Z produces "1" if and only if at least two bits in inputs A, B, C, D are 1s.

(1.a) Fill in the truth table for Z on the right.

(1.b) Write the minterm canonical form for Z, using Σ notation.

ABCD	Z
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

2 (15 points) Find the logic expression and fill in the truth table for the following circuit.



A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

3 (25 points) Binary arithmetic operations.

(3.a) Convert each of the following binary numbers to their decimal equivalent.

Unsigned Binary	Decimal
10110	
01011	

2's complement binary	Decimal
10111	
01001	

(3.b) Convert each of the following decimal numbers to 2's complement numbers.

Decimal	2's complement binary
20	
-27	

(3.c) Carry out the following additions and indicate if there is overflow for unsigned or 2's complement representations.

			Overflow (Yes/No)	
Addend	Augment	Binary result	Unsigned	2's compl
1011	1100			
1100	0101			

4 ***(15 points) Obtain a minimal sum-of-products (AND-OR) logic expression for the following function: Z(A,B,C,D)=Σ(0,1,2,8,9,13,15). Draw the simplified sum of products schematic using NAND-NAND implementation for Z.***

CD \ AB	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

5 ***(15 points) Obtain a minimal product-of-sums (OR-AND) logic expression for the following function: Z(A,B,C,D)=ΠΠ(4,5,8,10,12,14,15)+d(7,9,13). Draw the simplified product of sums (OR-AND) schematic for Z.***

CD \ AB	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

6 ***(15 points). Draw the output waveform at each gate output, /B, A*/B and Z in the following schematic on the grid space provided. Each gate has 10-time-unit delay. The grid interval is 10 time units.***