ECE 333

HW Set # 1

Solutions

FCE 333 Problem 1.1 Solutions

Given: A. Convert 23.625_{10} to binary

B. Convert 11011001.110101_2 to decimal

C. Convert $DEADBEEF_{16}$ to binary

D. Perform addition + subtraction. Are results correct?

6	0110	-8	1000	+3	0011	-3	1101
+-3	1101	+-8	1000	--4	1100	--4	1100

Solution: 23.625

A. $23/2 = 11$ r 1 ↓

$11/2 = 5$ r 1

$5/2 = 4$ r 1

$4/2 = 2$ r 0

$2/2 = 1$

10111.101_2

$.625 - 1/2(1) = .125$

$.125 - 1/4(0) = .125$ ↓

$.125 - 1/8(1) = 0$

B. 11011001.110101_2

$1\cdot1 + 0\cdot2 + 0\cdot4 + 1\cdot8 + 1\cdot16 + 1\cdot32 + 0\cdot64 + 1\cdot128 + 1\cdot256 = 441$

$1\cdot\frac{1}{2} + 1\cdot\frac{1}{4} + 0\cdot\frac{1}{8} + 1\cdot\frac{1}{16} + 0\cdot\frac{1}{32} + 1\cdot\frac{1}{64} = .828125$

441.828125_{10}

C. DEADBEEF$_{16}$

1101	1110	1010	1101	1011	1110	1110	1111$_2$
D	E	A	D	B	E	E	F

D.

```
   6        0110
 + -3       1101
          1|0011
           ↑
          c.o.
```

carry-out is same as cary-in to last bit
<u>Correct</u>

```
                 ←carry-in
             1 0
  -8          1000
+ -8          1000
            1|0000
```

carry-out is 1, carry-in to last bit is 0, overflow (-16 cannot be shown with 4-bits).
<u>incorrect</u>

```
                      2's comp.
   3     0011  ->    0011
 - -4    1100      + 0100
                   0|0111
```

carry-out is 0, same as carry-in to last bit
<u>correct</u>

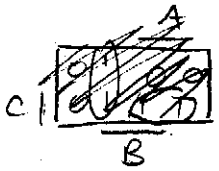
```
                        1
  -3    1101  ->      1101
 - -4   1100        + 0100
                    1|0001
```

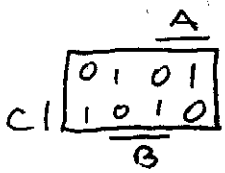
carry-out is 1, same as carry-in
<u>correct</u>

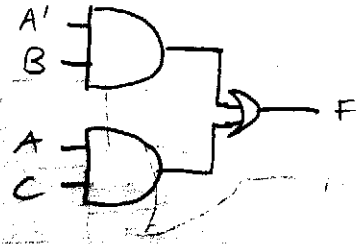
ECE 333 Problem 1.2 Solutions

A. $F(A,B,C) = A'B'C + A'BC' + AB'C' + ABC$

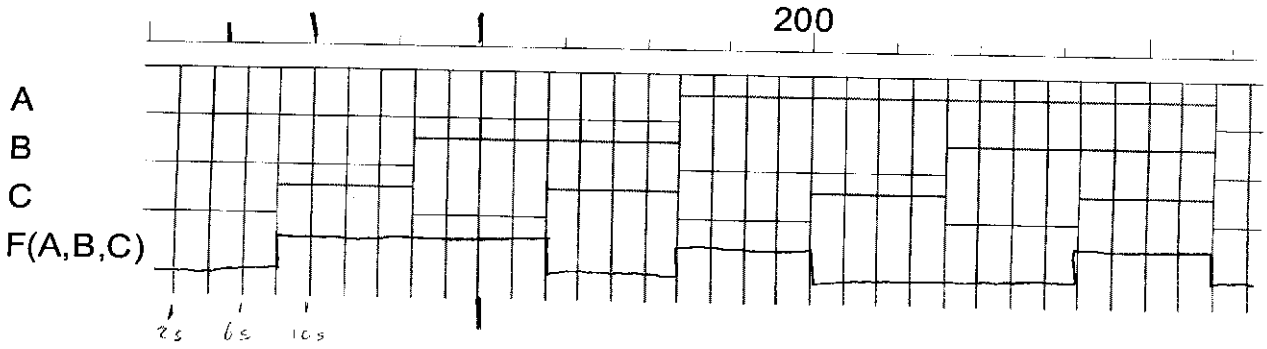
A B C	F
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1







Draw the output waveform for the circuit below. The reference grid in the timing diagram is one line per 10 units. Considering 10 units=2 seconds what is the clock period of signal A (T_A), signal B (T_B) and Signal C (T_c). What is the frequency of signal A?



$T_A = 160 \text{ units} \left(\frac{2\text{ s}}{10 \text{ units}}\right) = \frac{32}{64}\text{ s}$

$T_B = 80 \text{ units} \left(\frac{2\text{ s}}{10 \text{ units}}\right) = \frac{16}{32}\text{ s}$

$T_C = 40 \text{ units} \left(\frac{2\text{ s}}{10 \text{ units}}\right) = \frac{8}{16}\text{ s}$

$f_A = \frac{1}{T_A} = \frac{.0313 \text{ Hz}}{.062}$

.0156 Hz

Problem 1,2 cont'd Solutions

B. Convert $\Sigma(A, B, C) = A'(B+C) + B'(A+C')$ to Minterm canonical form

$= A'B + A'C + AB' + B'C'$

$= A'B(C+C') + A'(B+B')C + AB'(C+C') + (A+A')B'C'$

$= A'BC + A'BC' + \cancel{A'BC}^{\text{Dup.}} + A'BC' + AB'C + AB'C' + \cancel{AB'C'}^{\text{Dup}} + \cancel{ABC}^{\text{Dup}}$

(3) (2) (1) (5) (4) (0)

$\Sigma(1, 2, 3, 4, 5)$

C. Write compliment of $\Sigma(0, 1, 4, 8, 13, 15)$ in maxterm form

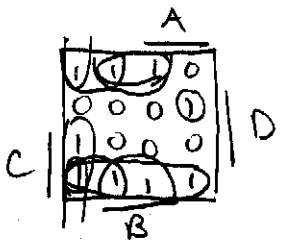
include all elements not used in minterm form

~~$\Pi(2, 3, 5, 6, 7, 9, 10, 11, 12, 14)$~~

$\Pi(0\ 1\ 4\ 8\ 13\ 15)$

ECE 130 Problem 1.3 Solutions

A. Convert $\Sigma(0, 2, 3, 4, 6, 9, 10, 12, 14)$ to minimal and-or logic

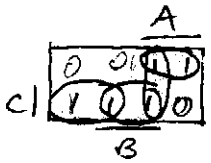


$A'B'D' + A'CB' + AB'C'D + BC'D' + CD'$

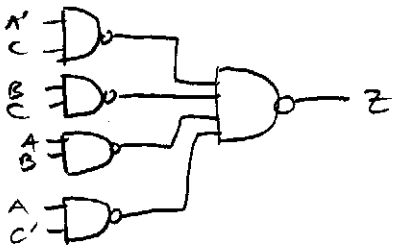
$CD' + CB'A' + A'C'D' + DC'D' + AB'C'D$
$AB'C'D + A'B'C + AD + BD' + CD'$

B. $Z(A, B, C) = \Sigma(1, 3, 4, 6, 7)$

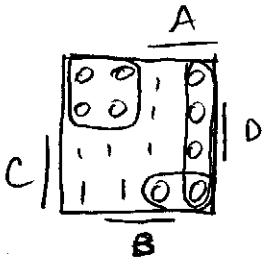
implement hazard-free form in NAND-NAND form



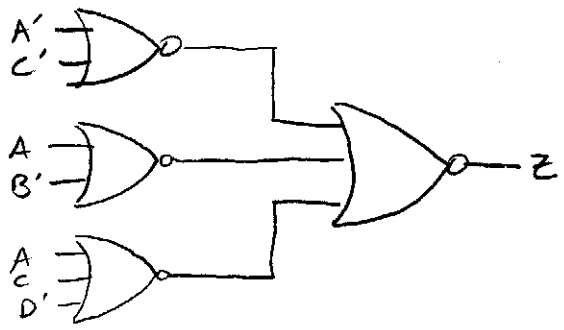
$\left((A'C)' \cdot (B \cdot C)' \cdot (A \cdot B)' \cdot (A \cdot C')'\right)'$



C. $Z = \Sigma(2, 3, 6, 7, 12, 13, 15)$ convert to NOR-NOR

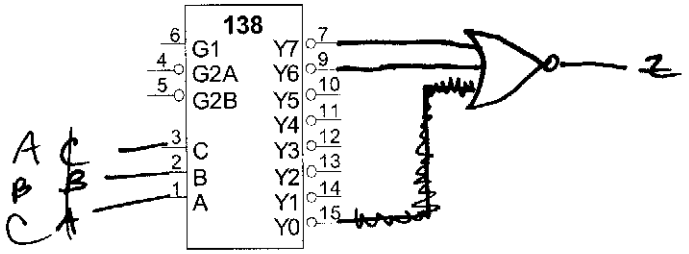


$\left((A + C)' + (A' + B)' + (A' + C' + D)'\right)'$



ECE 333 Problem 1.4 Solution

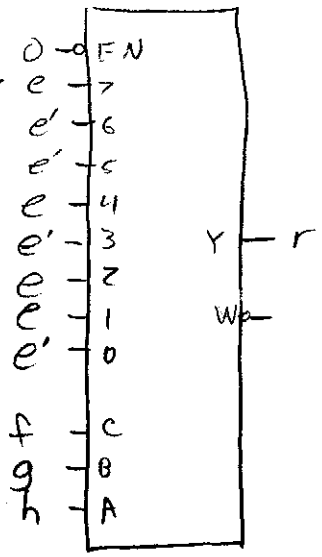
A. ~~(5 points)~~ Implement the logic function Z (A, B,C) = A'•(B+C) + B'(A+C') using the 3 to 8 decoder shown below. C is the most significant selection bit of the decoder. Use additional gates if necessary.



B. Multiplexor does not have enough inputs to directly connect 1's and 0's to it's inputs. simplify. use f, g, h as selection, and then e or e' as input.

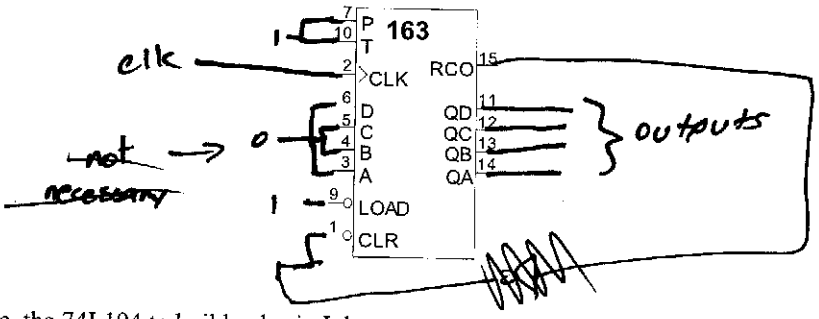
f g h	f e' e
0 0 0	1 0
0 0 1	0 1
0 1 0	0 1
0 1 1	1 0
1 0 0	0 1
1 0 1	1 0
1 1 0	1 0
1 1 1	0 1

choose e or e' where function should be 1

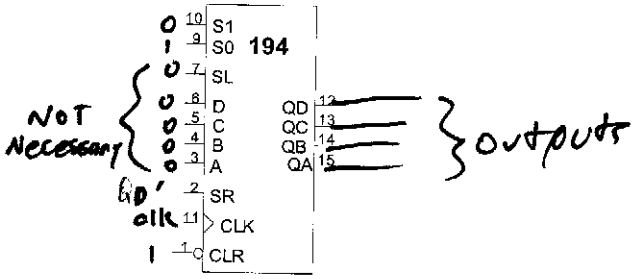


e f g	h	f
0 0 0	0	1
	1	0 h'
0 0 1	0	0
	1	h
0 1 0	0	0
	1	h
0 1 1	0	1
	1	0 h'
1 0 0	0	0
	1	h
1 0 1	0	1
	1	0 h'
1 1 0	0	1
	1	0 h'
1 1 1	0	0
	1	1 h

C. ~~**(5 points)**~~ Make the necessary connections to the 74LS163 counter to operate in the free running mode (from 0 to 15 and back). *The 74LS163 is a synchronous 4 bit binary counter. It has P and T inputs which enable counting when high, a clock input, a parallel load input (D-A) which is used when the LOAD input is low and a the clock The clear input loads zero into the counter and is also synchronous and active low. The RCO output goes high when the output is 15. The outputs, QD-QA, reflect the state of the counter.*



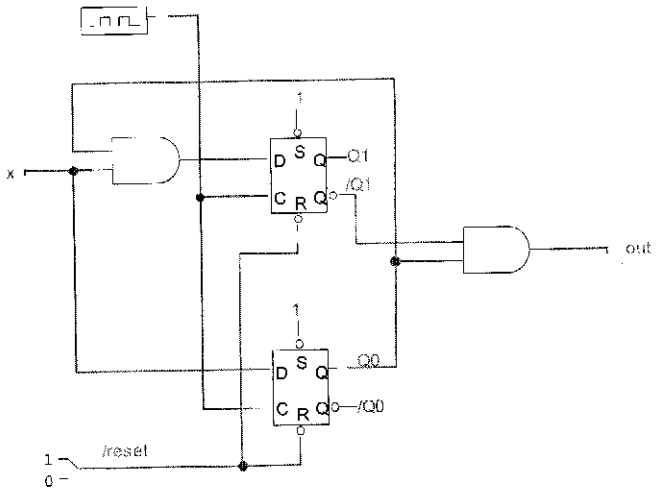
D. ~~**(5 points)**~~ Use the 74L194 to build a basic Johnson counter. An n-bit shift register with the complement of the serial output fed back into the serial input is a counter with 2n states and is called twisted ring, Moebius or Johnson counter. *The universal register 74LS94 uses a clock input, an active low clear input and two mode inputs. The modes are S1S0=00, hold, S1S0=01shift right (toward D),S1S0=10shift left (toward A) and S1S0=11, parallel load. R is the serial input for right shift and L is the serial input for left shift.*



ECE 333 Problem 1.5 Solution

Problem 5 ~~(20 points)~~ **(5 points)**

A. ~~(7.5 points)~~ **Analyze the following circuit.** Write the excitation and output equations, fill in the transition table and draw a state diagram for the state machine shown below. You may ignore the set and reset inputs for the purpose of your state diagram.



Q_1 = state 1

Q_0 = state 0

Excitation Equations

state 1

$$Q_1 = (x \cdot Q_0)$$

state 0

$$Q_0 = (x)$$

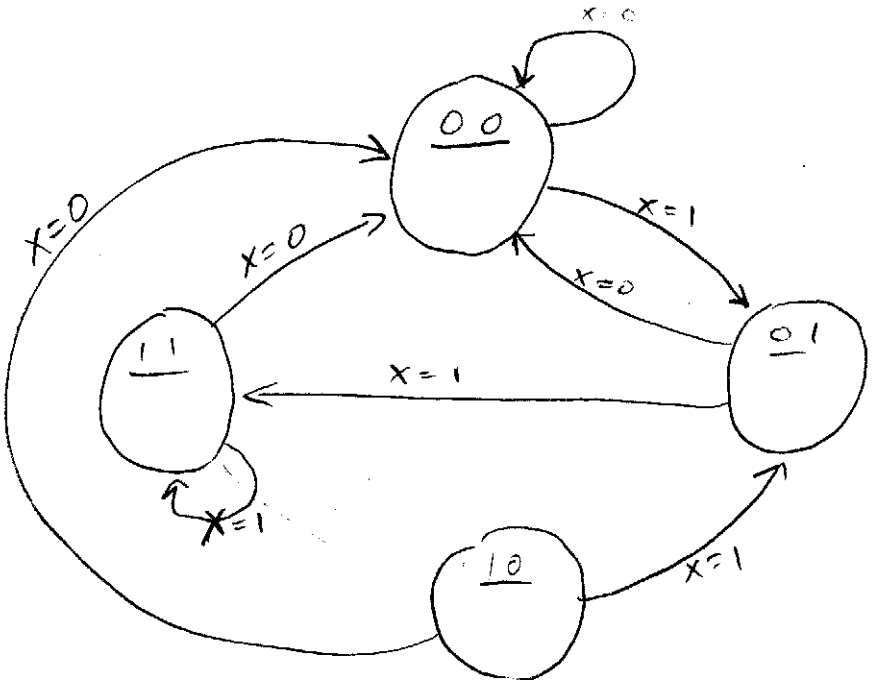
Output Equations

$$Out = (Q_0 \cdot Q_1')$$

transition table

state Q_1 Q_0	input x	Next state Q_1^* Q_0^*
0 0	0	0 0
0 0	1	0 1
0 1	0	0 0
0 1	1	1 1
1 0	0	0 0
1 0	1	0 1
1 1	0	0 0
1 1	1	1 1

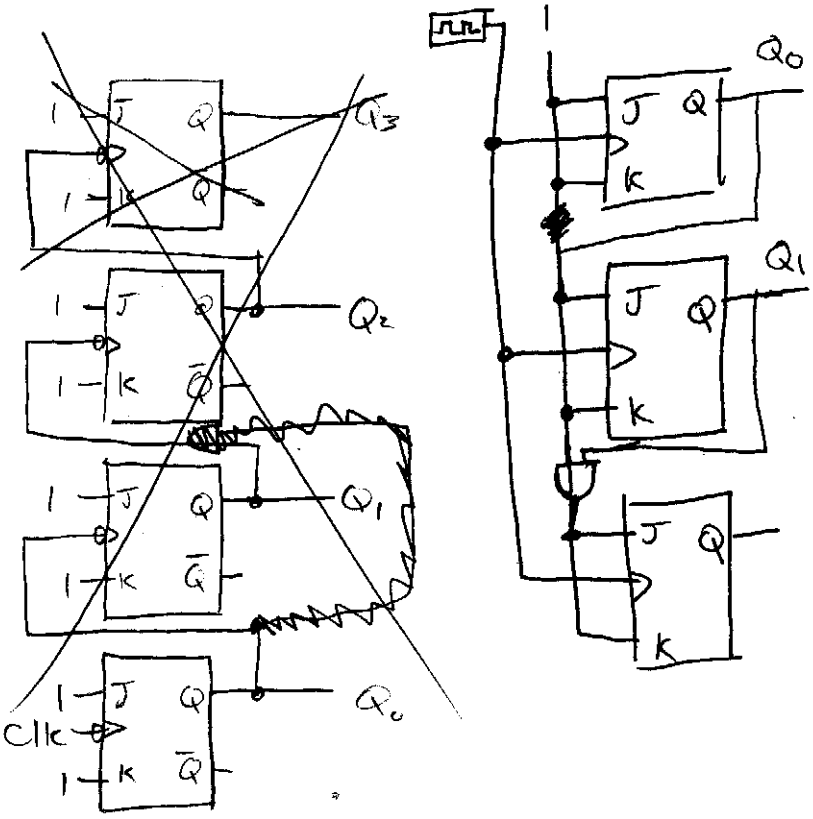
State Diagram



B. Design a synchronous 0-7 binary counter using JK Flip-Flops

J	K	Q_n
0	0	hold
0	1	~~reset~~
1	0	~~reset~~
1	1	change

JK Flip-Flops operate on falling edge of clock cycle so we can simply hook them up like this.



Problem 1.5 cont'd Solutions

c.

combinations of last 2 inputs:

0 0	state A
0 1	state B
1 0	state C
1 1	state D