ECE 333
Winter 2003-2004
Exam #1

This exam is closed-notes and closed-book. You may use your brain and a writing instrument.

"To the best of my knowledge and on my honor as a student and as a professional, I attest that I have not acted in any way that could be considered academic misconduct (e.g., cheating) either in the preparation for or in the taking of this exam."

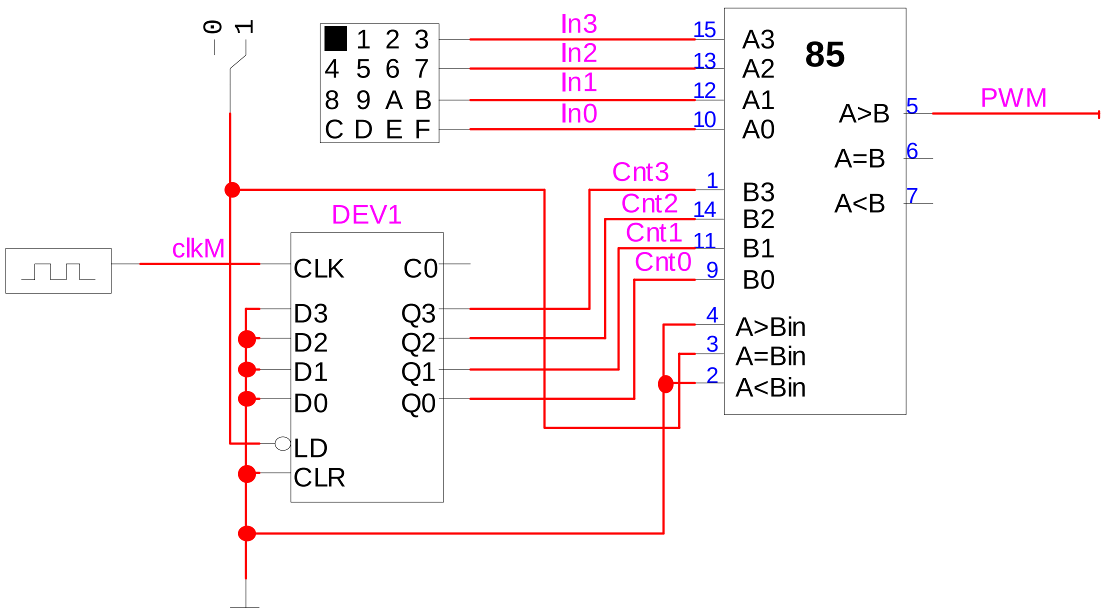
Signature:

Name:

Point allocation:

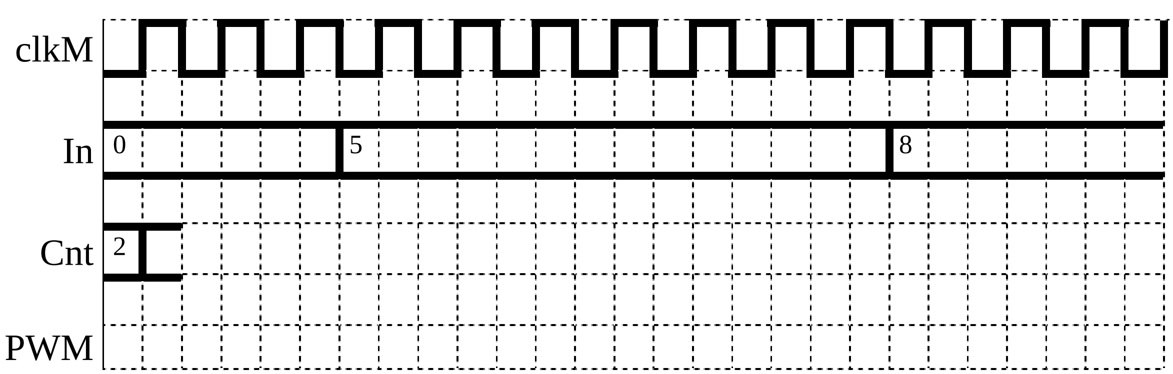
1. Your friend has observed that the largest source of noise in the PWM DAC is the rippling growth and decay that occurs at the output filter. This ripple has the same frequency as the PWM-frequency with the growth occurring during the high portion of the output and the decay occurring during the low portion of the output. She has hypothesized that she can decrease this noise by rearranging the PWM signal into a signal that alternates high and low, but with the same overall duty-cycle. She has designed an improved PWM-DAC to test this theory. Having absolutely no digital ability (she didn't think that "digital systems" was an important class), she has turned to you for help in testing her theory.

Below is a schematic for the PWM designed in lab #3:

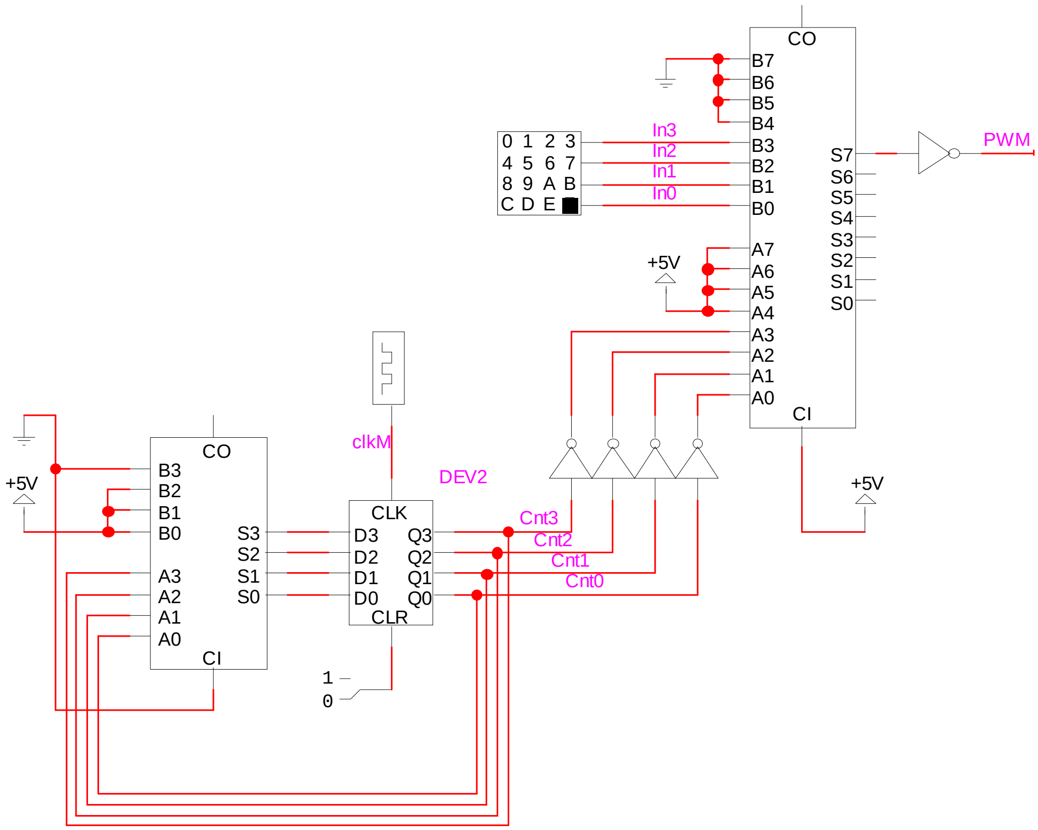


In the above schematic, clkM is the input master clock, DEV1 is the 4-bit counter, the LS85 chip is the comparator (with PWM output A>B) and a hex keyboard is used as the digital input. A switch is used to reset the counter's state.

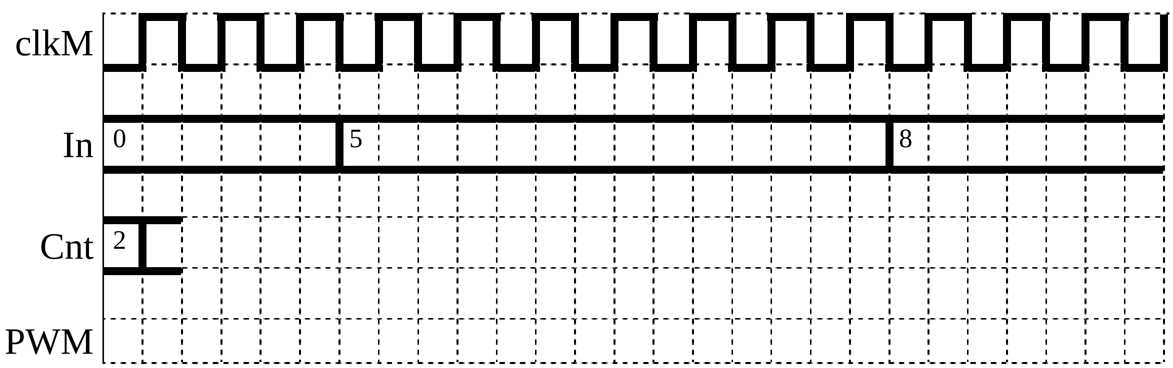
Complete the following timing diagram for the above PWM circuit. Use hexadecimal values for busses (In and Cnt). In3 and Cnt3 are the MSBs.



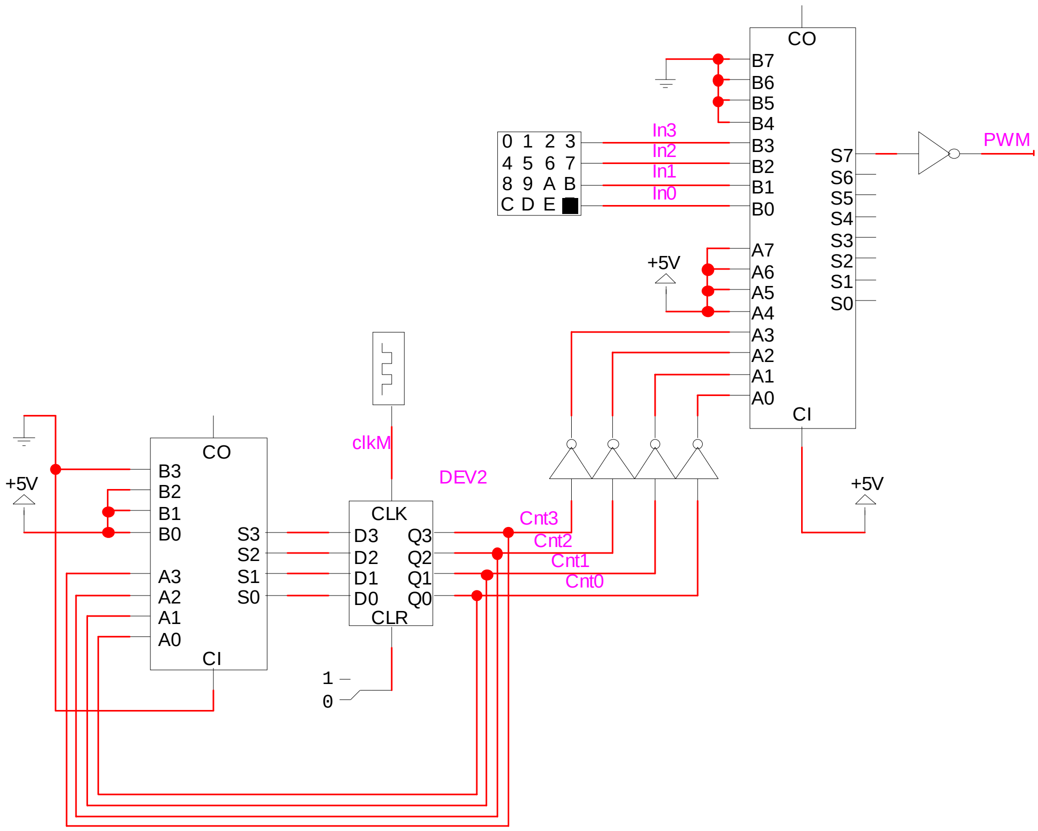
Now consider your friend’s circuit:



Here, a 4-bit adder, a 4-bit register (DEV2), and an 8-bit adder are used together to form the PWM output. As before, complete the following timing diagram for the above circuit:



2. Write the Verilog code for your *so-called* friend's circuit (a blank sheet is provided on the following page). Since there are three blocks in the circuit, you should have three distinct sub-circuits in your code. However, you should feel free to optimize these sub-circuits with your buff Verilog skills.



```
module whackyPWM( In, clk, Cnt, PWM );

endmodule
```

3. You are shown the following simulation output from a Verilog module (next page). The module is supposed to function as a 4:1 multiplexer. It has inputs **d**, **c**, **b**, and **a**, select **[1:0] S**, and output **out**. When **S = 0**, **out** is supposed to be **a**. When **S = 1**, **out** is supposed to be **b**. etc.

You don't have access to the Verilog for the module, nor the test-bench code, but you still need to evaluate the quality of this module (you think it may have been written by a certain ex-friend of yours). Annotate the following timing diagram and decide whether or not you should send this module back to the designer. Explain your decision below.