ECE 333-02 (Laflen)
Exam 3

This exam is open-source, but each student must complete his/her own work. You will have three hours to complete this exam.

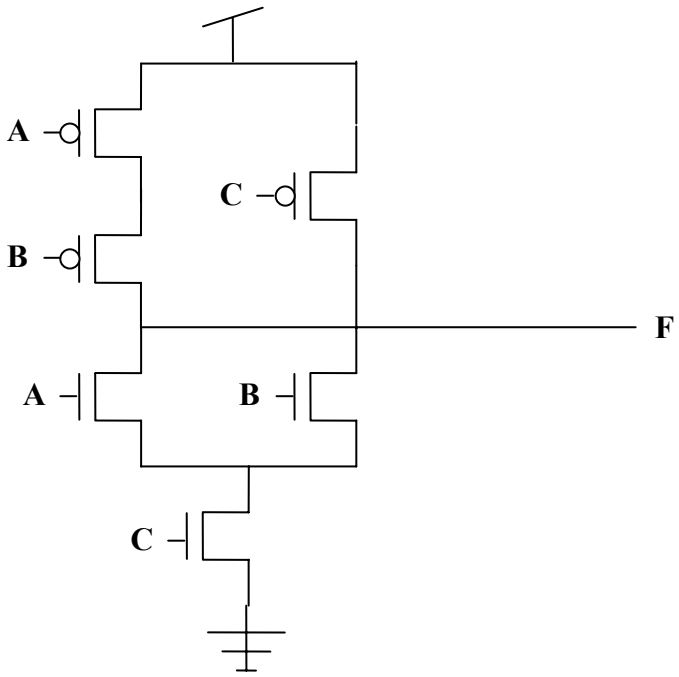
Please indicate agreement with the following statement by signing below:

"On my honor as a student, the work in this exam is my own."

Signature:

Name (Print):

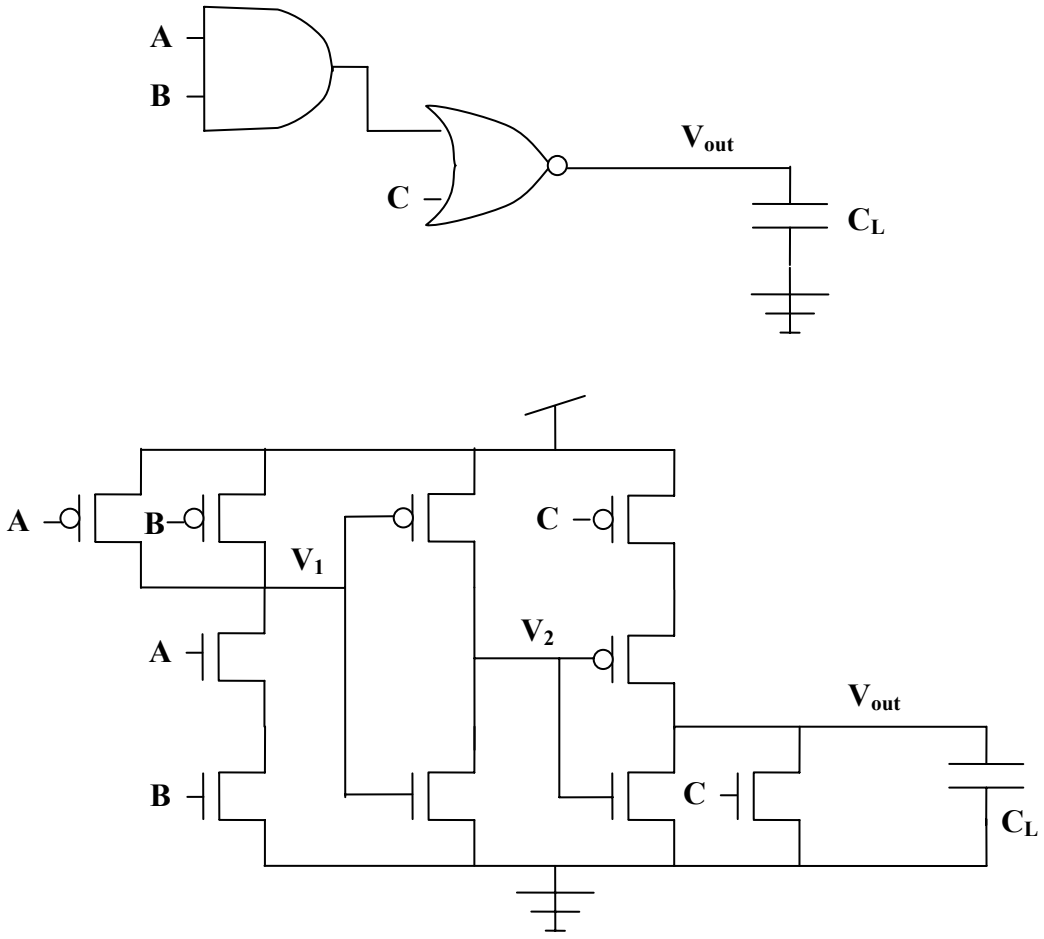
1.A. Derive the logical function associated with the following circuit:



1.B. Draw a circuit diagram for this function using only NAND, NOR, and INVERTER gates.

1.C. How many transistors are required for the NAND/NOR/INVERTER circuit?

2. A logical circuit and its transistor-level analogue are shown in the diagram below:

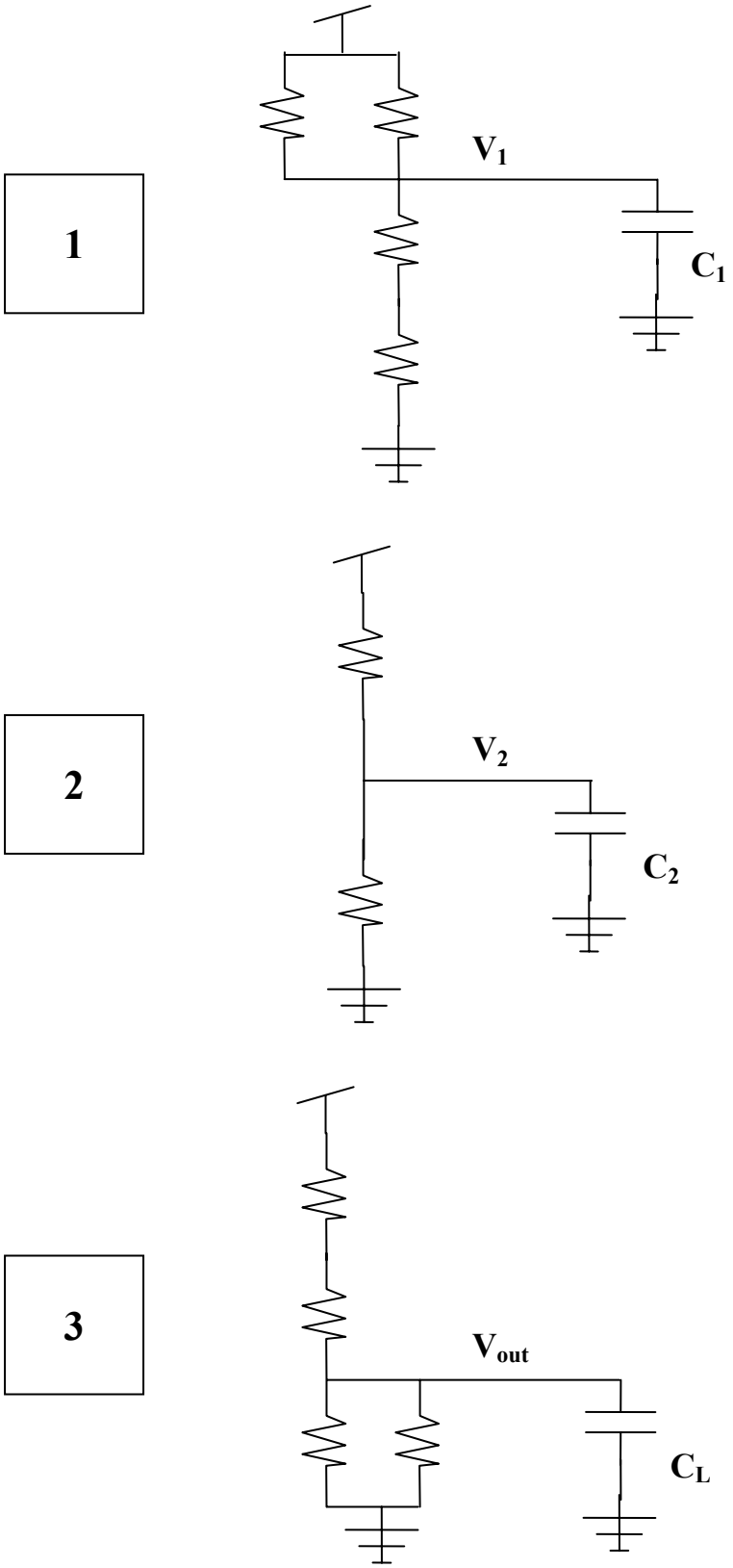


2.A. Divide the transistor circuit above into three sub-circuits (gates) and group these sub-circuits into two circuits corresponding to the two logical gates shown above. Clearly label each of the three sub-circuits, as well as the two larger circuits, with appropriate logical gate names.

2.B An RC-circuit template for the three sub-circuits from the previous transistor circuit is located on the following page. Assume that the inputs are $A=V_{dd}$, $B=V_{dd}$, $C=0$, and that these values have been constant for a long time.

1. **Write the appropriate resistor values next to each resistor on the template, assuming that an NFET is equivalent to R_L when "on" and R_H when "off" and that a PFET has twice these values.**

2. **Calculate the load capacitances C_1 and C_2 assuming that the gate capacitance for a PFET is C_P and the gate capacitance for an NFET is C_N.**


1
V1
C1
2
V2
C2
3
Vout
CL

2.C By making a few simplifying assumptions, you will now calculate the approximate total propagation delay for this circuit when the input A switches from V_{dd} to ground:

- **Assume that transitions within each sub-circuit are governed by an equation of the form**

$$V(t) = Ae^{-(t-\zeta)/\tau} + B$$

  when it is transitioning and that the output is constant before and after the transition.

- **Assume that each transistor switches instantaneously between "on" and "off" when the input voltage changes sufficiently according to the following rule:**
  - **The transistor will switch when the input voltage drops from V_{dd} to V_{IL}.**
  - **The transistor will switch when the input voltage rises from ground to V_{IH}.**
  - **$V_{IH} > V_{IL}$**
  - **The transistor exhibits hysteresis.**
- **Assume that when a transistor is "off" its equivalent resistance is so high that it can be approximated as an open circuit.**

The approximate total propagation delay for this circuit is the amount of time it takes from the transition in A (to either V_{IL} or V_{IH}) to a corresponding transition in V_{out} (to either V_{IL} or V_{IH}).

A second RC-circuit template for the three sub-circuits is provided at the end of this section. You may use this template to help you calculate the following information:

1. **Determine the lumped RC time constant that governs the transitions in each sub-circuit:**

   a. $\tau_1 =$

   b. $\tau_2 =$

   c. $\tau_3 =$

2. **Determine the parameters A and B for each sub-circuit:**

   a. $A_1 =$ $B_1 =$

   b. $A_2 =$ $B_2 =$

   c. $A_3 =$ $B_3 =$

   It may help to calculate the logical outputs of each sub-circuit so that you will know whether the final output should be high (V_{dd}) or low (0).

3. **Assume that input A reaches V_{IL} at time t_0. Let t_1 be the time at which V_1, the output of sub-circuit 1, reaches the voltage necessary to trigger a switch in sub-circuit 2 (e.g., either V_{IL} or V_{IH}), and so forth with t_2 and t_3. t0, t1, and t2 are the constants ζ in the above transition equation. Write the transition equations for each sub-circuit in terms of V_{dd}, V_{IL}, V_{IH}, τ_1, τ_2, τ_3, t_0, t_1, t_2, and t_3:**

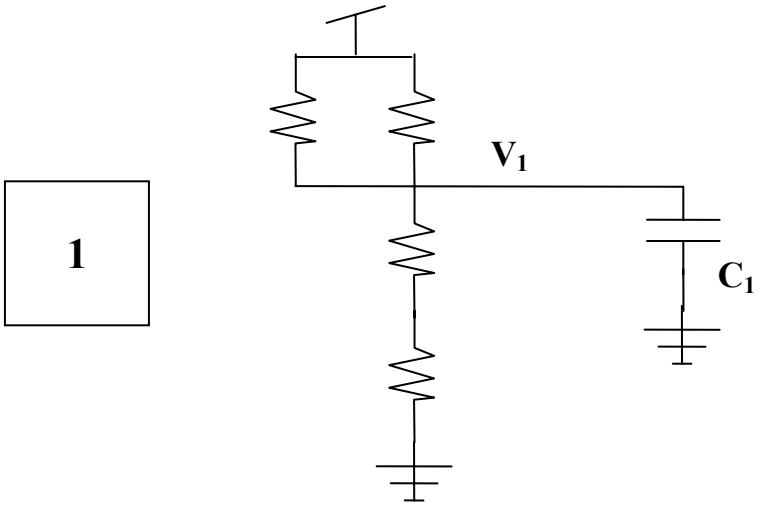
   a. **$V_1(t)$ =**

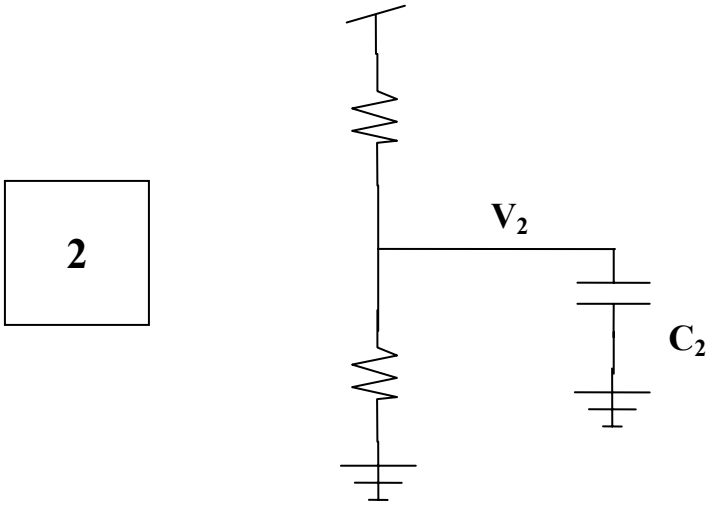
   b. **$V_2(t)$ =**

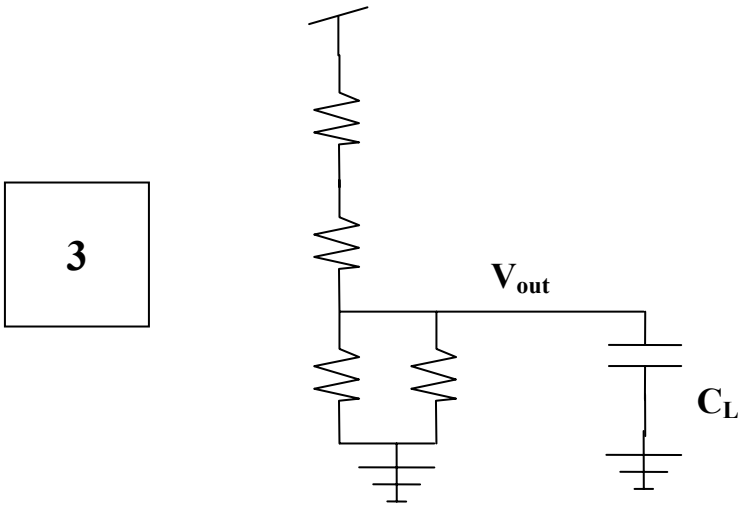
   c. **$V_{out}(t) = V_3(t)$ =**

4. **Use your transition equations to solve for t1, t2, and t3 in terms of R_L, C_P, C_N, C_L, V_{dd}, V_{IH}, V_{IL}, t_0, t_1, t_2, and t_3.**

5. **Assume $R_L = 10\ \Omega$, $C_P = C_N = 100$ fF, $C_L = 10$ pF, $V_{dd} = 5$ V, $V_{IH} = 4$ V, $V_{IL} = 1$ V, and $t_0 = 0$ s. What is the approximate total propagation delay for this circuit? Note that this is a conservative value because it assumes no transition in the FETs prior to activation.**


1
V1
C1


2
V2
C2


3
Vout
CL

2.D. The above circuit requires 10 transistors but can be implemented with less. Design a transistor-level circuit that uses only 6 transistors to accomplish the same task.

2.E. Calculate the approximate propagation delay for the 6-transistor circuit.

2.F. Draw a PLA for the same logical functionality of the above circuits.

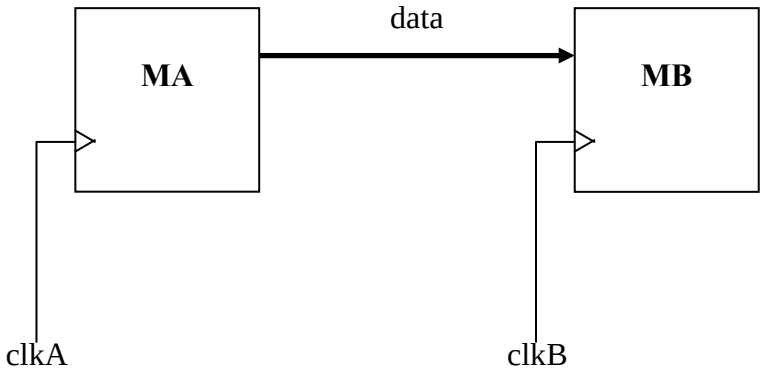
2.G. Will the PLA propagation delay be longer or shorter than the 10-transistor implementation? Explain.

2.H. Will the PLA propagation delay be longer or shorter than the 6-transistor implementation? Explain.

3.A. Draw a schematic of a pulse-width-modulation (PWM) logical unit that accepts a clock input "clk" and a 5-bit digital input "In" and produces a 1-bit PWM output "PWM."

3.B. If the clock frequency is *f* Hz, what is the periodic frequency of the PWM output (assuming that the digital input is held constant)?

4. Consider a system like the one below:



What could happen if clkA and clkB have the same frequency but are out of phase?

What could happen if clkA and clkB have a frequency mismatch?

Suggest a radical alteration to the above system that will insure the system against the issues listed above. Assume that the data conduit is purely digital (i.e., it is short and exhibits high noise immunity).