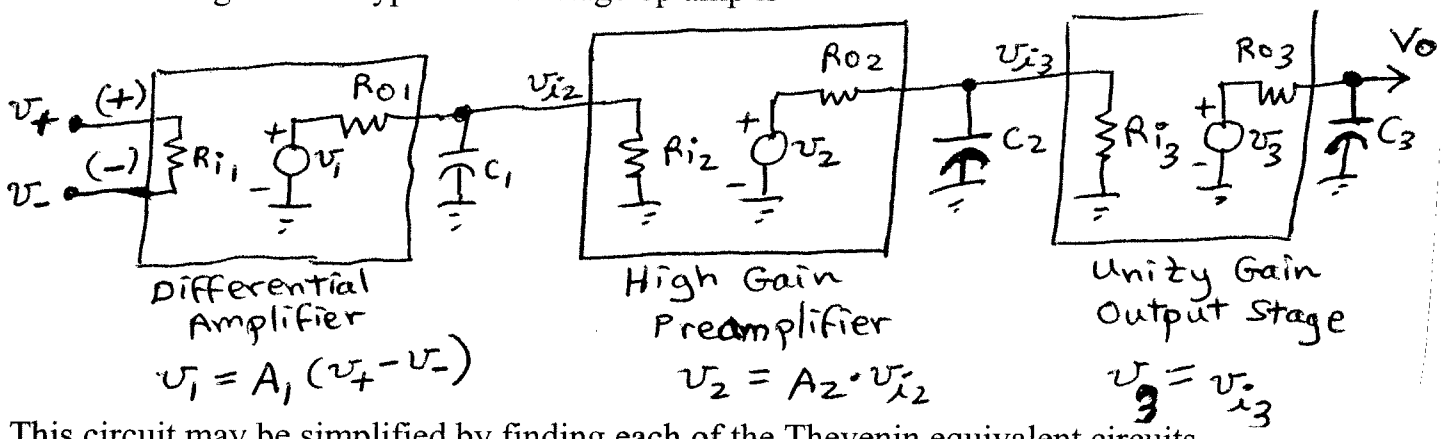
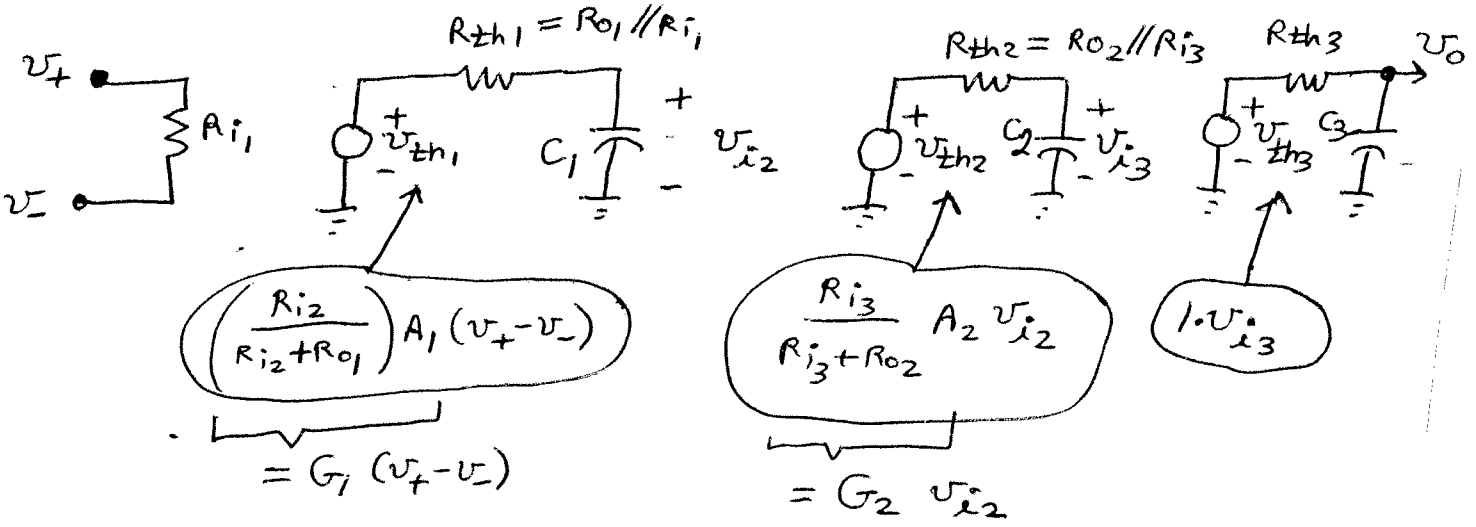
Operational Amplifier Frequency Response and Closed-Loop Stability

A real (open-loop) op amp is generally composed of three stages: a moderate-gain differential amplifer stage with high input resistance, a high-gain voltage preamplifier stage, and a unity-gain emitter-follower output stage with low output resistance. Each of these stages has an output resistance and also a ("parasitic", or unwanted) capacitive load. Thus each stage contributes significant voltage or current gain to the overall op amp operation, but also an (unwanted) first-order LPF RC filter section! Thus the voltage gain of a real op amp is NOT independent of frequency, as assumed in our ideal op amp model, but instead the voltage gain of a real op amp decreases with frequency.

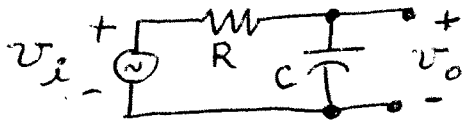
The block diagram of a typical three-stage op amp is



This circuit may be simplified by finding each of the Thevenin equivalent circuits seen "looking out from" the terminals of each capacitor, as shown below:



Earlier in this course we have shown that the simple first-order RC lowpass filter section

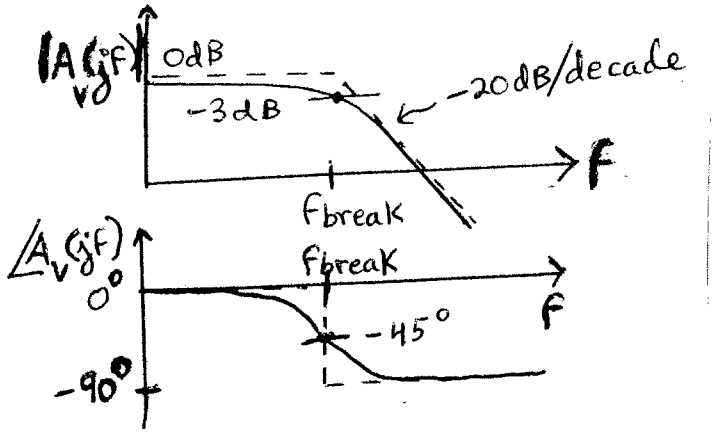


has the following transfer function:

$$Av(jf) = \frac{Vo(jf)}{Vi(jf)} = \frac{\frac{1}{(j\cdot 2\cdot\pi\cdot f\cdot C)}}{\frac{1}{(j\cdot 2\cdot\pi\cdot f\cdot C)} + R} = \frac{1}{1 + j\cdot 2\cdot\pi\cdot f\cdot R\cdot C} = \frac{1}{1 + \frac{jf}{f_{break}}}$$

$$\text{where} \qquad f_{break} = \frac{1}{2\cdot\pi\cdot R\cdot C}$$

Recall that wehave found that its magnitude and phase Bode plots are



Because the 3-stage op amp consists of a cascade of three first-order LPF sections (with voltage gains in between), its transfer curve must be given by

$$Av(jf) = \frac{Vo(jf)}{Vplus(jf) - Vminus(jf)} = \frac{G_1\cdot G_2\cdot 1}{\left(1 + \frac{j\cdot f}{f_1}\right)\cdot\left(1 + \frac{j\cdot f}{f_2}\right)\cdot\left(1 + \frac{j\cdot f}{f_3}\right)}$$

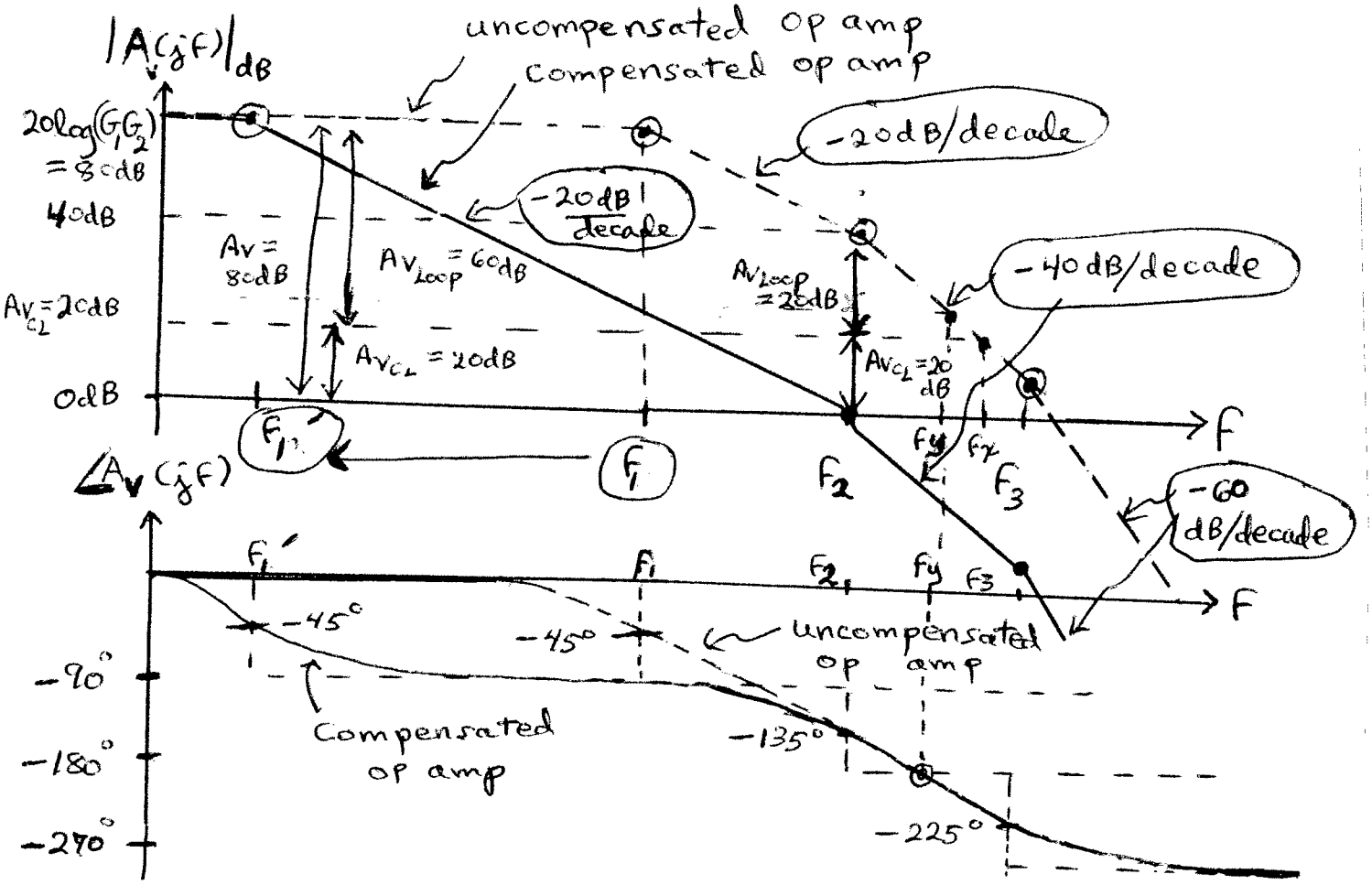
where the three break frequencies are

$$f_1 = \frac{1}{2\cdot\pi\cdot Rth_1\cdot C_1} \qquad f_2 = \frac{1}{2\cdot\pi\cdot Rth_2\cdot C_2} \qquad f_3 = \frac{1}{2\cdot\pi\cdot Rth_3\cdot C_3}$$

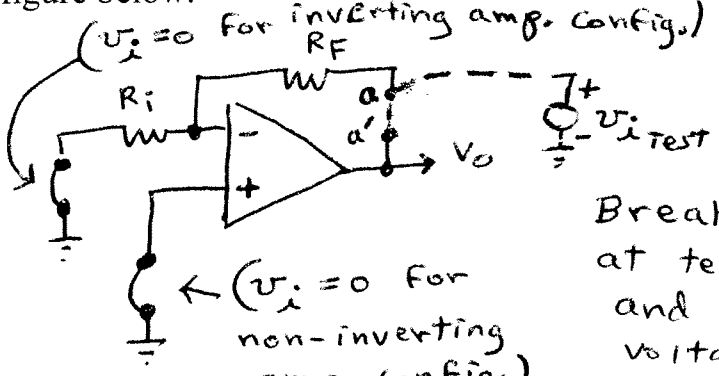
Typically, it is found that f_1 is the smallest, and f_3 is the largest, so the magnitude and phase of the (uncompensated) op amp's transfer function, |Av(jf)| and <Av(jf), may be plotted as the dotted curves shown below:

Phase and Magnitude Bode Plots for a typical 3-Stage Op Amp

(the uncompensated case is shown by dashed lines and the compensated case is shown by the the solid lines.)



If this (uncompensated) op amp is connected in *either* the *inverting* or the *non-inverting* amplifier configuration, then the gain around the feedback loop (called the "loop gain" Av_{LOOP}), may be found using Linear Superposition by setting the external input voltage, vin(t), to zero. This makes the two op amp amplifier configurations *identical*, as can be seen in the figure below.



Break feedback path at terminals a-a' and insert test voltage source "$v_{i\,test}$"

$$Av_{Loop} \triangleq \frac{v_o}{v_{i\,test}}$$

The loop gain Av_{LOOP} is defined by breaking the feedback loop anywhere, say at terminals a - a', and inserting a test voltage source, vi_{TEST}, between the input terminal and ground and measuring the voltage gain around the broken feedback loop. From the figure above, we see that

$$Av_{LOOP}(jf) = \frac{vo}{vi_{TEST}} = \frac{-R_I}{R_I + R_F} \cdot Av(jf) = -\beta \cdot Av(jf)$$

Where $\beta = R_I / (R_I + R_F)$ is the voltage gain of the external feedback network that is formed by the resistive voltage divider consisting of resistors R_I and R_F, and it is less than unity. β is often referred to as the "*return gain*". The minus sign must be used to account for the fact that the output is multiplied by β and then fed back into the op amp through its inverting (-) input.

The concept of loop voltage gain is important from a stability standpoint in any "closed-loop" feedback system, because it indicates whether there are any frequencies at which the system will oscillate, which is clearly an undesirable condition in an amplifier!

There are two "Barkhausen conditions" that must simultaneously be satisified if a feedback system is going to oscillate at a given frequency "f":

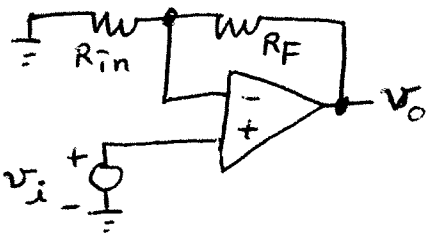
1. The magnitude of the voltage gain around the loop at frequency "f" must have a magnitude which is equal to or greater than unity. This will allow any sinusoidal noise component at frequency "f" in the circuit (all frequencies are present in the startup transient pulse, as the circuit is first powered up) to become larger and larger as it propagates around the feedback loop and thus small noise sinusoid can build up into a large, sustainable oscillation at frequency "f".

$$\left| Av_{LOOP}(jf) \right| \geq 1$$

2. The phase angle of the voltage gain around the loop at frequency "f" must be an integral multiple of 360 degrees (or 2π radians), so that the (sinusoidal) noise that travels around the feedback loop at frequency "f" arrives back at the input in phase with the sinusoidal noise that is already there, so constructive interference will occur and therefore allow oscillations at frequency "f" to build up.

$$< Av_{LOOP}(jf) = \quad n \cdot 2 \cdot \pi$$

Let us consider the standard non-inverting op amp negative-feedback amplifier configuration shown below. (Analysis of the inverting op amp amplifier configuration would proceed in similar fashion and lead to nearly identical results.) The closed-loop voltage gain Av_{CL} = vo/vi may be found by writing vo in terms of the feedback ("return") gain β as shown:



$$v_o = Av\cdot(vplus - vminus) = Av\cdot\left(vi - \beta\cdot v_o\right) \qquad \text{where} \quad \beta = \frac{Rin}{Rin + R_F}$$

Thus

$$v_o\cdot\left(1 + Av\cdot\beta\right) = vi\cdot Av \qquad (\beta = \text{"return gain"})$$

Therefore $$Av_{CL} = \frac{vo}{vi} = \frac{Av}{1 + \beta\cdot Av}$$

For $\beta\cdot Av >> 1$, $$Av_{CL} = \frac{1}{\beta} \quad \text{(Approximately)}$$

Dividing both sides of the inequality above by the return gain, β

$$\text{For } Av >> \frac{1}{\beta} = Av_{CL}$$

Thus as long as the open-loop gain Av is sufficiently greater than $1/\beta = (Rin + R_F) / Rin$, which is the closed-loop gain that the op amp has been "strapped for", the actual voltage gain of circuit is fairly accurately predicted by the ideal op amp formula $Av = (Rin+R_F)/Rin$. (Perhaps a good rule of thumb is to require Av to be at least 2 times greater than Av_{CL}.) Note that the closed-loop gain depends mainly on the feedback resistors Rin and R_F and NOT very much on the open-loop gain Av! This is fortunate, since the feedback resistors Rin and R_F can be made much more stable (over time, temperature, power supply variations, etc.) than can the open-loop gain of the op amp, Av!

Also note from the result above that for $\beta * Av >> 1$

$$Av_{CL} = \frac{Av}{1 + \beta\cdot Av} = \frac{A_v}{\beta\cdot Av} = \frac{Open\_Loop\_Gain}{|Loop\_Gain|} = \frac{Av}{|Av_{LOOP}|}$$

Thus $$|Av| = |Av_{CL}|\cdot|Av_{LOOP}|$$

When these voltage gains are expressed in dB (as on a Bode Plot)

$$20\cdot\log(|Av|) = 20\cdot\log(|Av_{CL}|\cdot|Av_{LOOP}|) = 20\cdot\log(|Av_{CL}|) + 20\cdot\log(|Av_{LOOP}|)$$

$$Av_{dB} = Av_{CLdB} + Av_{LOOPdB}$$

Note from the Bode plot of the uncompensated op amp shown above that if the op amp is strapped for a closed-loop voltage gain of 20 dB (or a gain of 10, with Ri = 1 kΩ and Ri = 9 kΩ), then at a frequency well below the first break frequency f_1, the closed-loop gain is 20 dB, and the loop gain is 60 dB. However, at the second break frequency, f_2, the closed-loop gain is still 20 dB, but now the loop gain has fallen to only 20 dB. As we go to higher frequencies, we eventually arrive at frequency fx where the 20 dB horizontal line (representing the desired closed-loop gain) is intercepted by the descending open-loop gain line. At this frequency (fx) the amplifier no longer exhibits a 20 dB closed-loop voltage gain, since the loop gain has fallen to 0 dB (unity gain), and therefore this intercept frequency "fx" approximately represents the high frequency limit of this 20 dB amplifier.

However there is a BIG problem with this circuit, because strapping this uncompensated amplifier for a closed-loop voltage gain that is too low (such as 20 dB) makes it oscillate, and thus become unstable! This circuit will break into undesired oscillations at the frequency "fy" (see the phase plot).

This is because the open-loop gain phase plot ($<Av$) passes through -180 degrees at the frequency fy. Therefore, at this same frequency fy, the phase of the loop gain ($<Av_{LOOP}$) must be -180 + (-180) = -360 degrees, since passing through the (-) input of the op amp automatically adds another -180 degrees to the phase of the signal. Furthermore, at this frequency fy, we can see that the magnitude of the loop gain is still >> 1. Therefore, the two Barkhausen criteria are satisfied at frequency fy, and undesired oscillations will therefore develop at this frequency!

But now let us consider strapping the amplifier for a higher closed-loop gain. Say, 40 dB. From the horizontal "40 dB" dotted line on the figure above, we see that the useable bandwidth has been reduced from "fy" to "f_2", but now the loop gain is WELL BELOW unity at frequency "fy", where the phase of the open-loop gain of the op amp reaches the "possible oscillation value" of 180 degrees. In fact, because frequency f_2 corresponds to the second break frequency of the op amp, the phase shift at this frequency, which is the frequency where the loop gain (Av_{LOOP}) of the op amp is unity, is only approximately -135 degrees, and thus we are operating with a phase shift at unity gain that is a comfortable 180 - 135 = 45 degrees away from the problem value of 180 degrees! Thus when we strap this uncompensated op amp for a gain of 40 dB, the uncompensated op amp will be stable, with a "phase margin" of 45 degrees. It is always a good idea to operate an amplifer with a suitable phase margin to ensure that subsequent changes in component values due to aging, power supply variation, temperature change, etc. do not allow the circuit to become unstable at a later time.

The op amp may be "compensated" to make it *unconditionally stable,* no matter what closed-loop gain it is strapped for. Let us consider the worst-case possible feedback situtation from the standpoint of stability considerations, which is when the amplifier is strapped for a closed-loop voltage gain of unity (as in the non-inverting unity-gain voltage follower configuration). Under this condition, the loop gain $|Av_{LOOP}|$ will be as high as possible, and in fact it is equal to the closed-loop gain magnitude |Av|. Assuming that a 45 degree phase margin is desired, we look at the loop gain of the uncompensated op amp at frequency f_2, and we see it is 40 dB instead of being equal to or less than unity as desired!)

This problem is solved by adding a compensation capacitor between the output node of the differential amplifier stage of the op amp, in parallel with the parasitic capacitance C_1 that lowers break frequency f_1 down to f_{1new}, where f_{1new} is chosen so that the 20 dB/decade slope in the open-loop voltage gain |Av(jf)| reaches unity gain at the second break frequency f_2. Thus at break frequency f2, where the phase has only fallen to -135 degrees, and is thus 45 degrees away from problem frequency "fy" where the phase is -180 degrees, the loop gain has already fallen to unity. Thus there is NO CHANCE of oscillation, no matter what closed-loop gain the amplifier is strapped for since at the 180 degree phase shift frequency, the voltage gain magnitude has to be considerably less than unity. Unfortunately, unconditional stability is bought at the high price of drastically reduced bandwidth of the op amp. Most modern medium-bandwidth op amps are internally compensated, such as the 741 and the TL-072. However, in order to attain wider operating bandwidth, some "high frequency" op amps (such as the TLE2037) are left uncompensated, allowing the user to operate them at higher closed-loop voltage gains, providing that the user adds the appropriate compensating capacitor based upon the closed-loop gain they are strapping the op amp for so that they can operate their amplifer in its stable region with a suitable phase margin.

Note that if the compensated op amp is strapped for a unity closed-loop voltage gain, its useable bandwidth (upper frequency limit) is approximately "f_2". Therefore, the second break frequency "f_2" is called the "*unity gain bandwidth*" of the op amp, and this value is specified as an op amp parameter in the data sheet of an op amp. Furthermore, since the slope of the open-loop gain |Av(jf)| is approximately -20 dB/decade throughout its useable frequency range, if we strap the amplifer for a closed-loop voltage gain of 10 (20 dB), the bandwidth decreases by 20 dB (a factor of 10) to $0.1*f_2$. If we strap it for a closed-loop voltage gain of 100, then the bandwidth (BW) decreases another 20 dB (factor of 10) to $0.01*f_2$. Clearly the product of the closed-loop gain and the useable bandwidth of the resulting amplifer must approximately equal f_2, the unity gain bandwidth.

$$Av_{CL} \cdot BW = f_2 = \text{Unity\_Gain\_BW} = \text{Gain\_Bandwidth\_Product}$$

For this reason, the "u*nity gain bandwidth*" parameter of an op amp is also called its "*gain-bandwidth product*". The published gain-bandwidth product for an LM741 amplifer is 1 MHz, the TL-072 (available from our instrument room) is 3 MHz, and the TLE2037 has a gain-bandwidth product of 85 MHz!

Ex #1: An internally-compensated TL-072 op amp is strapped for a closed-loop voltage gain magnitude of 10, 100, and 1000, using either the inverting or the non-inverting amplifier configuration. It has a gain-bandwidth product of GBW := 3·MHz. Find the useable bandwidth (upper frequency limit) in each case:

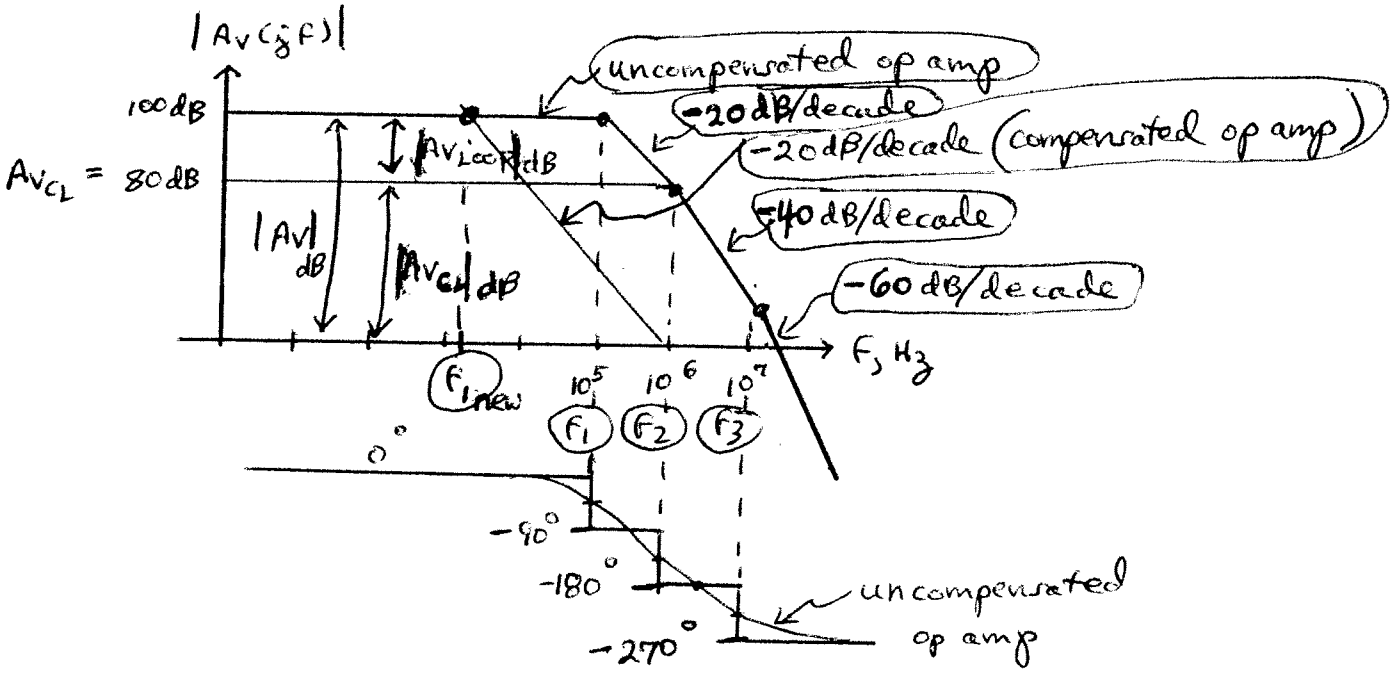
for $Av_{CL} := 10$ $BW := \frac{GBW}{Av_{CL}}$ $BW = 300 \times 10^3\,Hz$

$Av_{CL} := 100$ $BW := \frac{GBW}{Av_{CL}}$ $BW = 30 \times 10^3\,Hz$

$Av_{CL} := 1000$ $BW := \frac{GBW}{Av_{CL}}$ $BW = 3 \times 10^3\,Hz$

Ex #2: An uncompensated op amp exhibits a dc open-loop voltage gain of $Avdc := 10^5$ =100 dB, and has break frequencies $f1 := 10^5 \cdot Hz$, $f2 := 10^6 \cdot Hz$, and $f3 := 10^7 \cdot Hz$. What is the minimum permissible closed-loop voltage gain for which this amplifier may be strapped and still be stable to within a 45 degree phase margin? What is its useable bandwidth at this minimum permissible closed-loop voltage gain? If it is strapped for a gain below this critical level, at what precise frequency will the circuit oscillate?

From the sketch of |Av(jf)| and <Av(jf) below, we see that $|Av_{LOOP}|$ falls to 0 dB (unity) at f_2 = 1 MHz, where the |Av(jf)| is approximately 80 - 3 = 77 dB, since at a break frequency (f_2), the true gain curve should be approximately 3 dB below the Bode asymptote line.



To find this value more precisely, we may construct its transfer function:

$$Av(f) = \frac{10^5}{\left(1 + j\cdot\frac{f}{10^5}\right)\cdot\left(1 + j\cdot\frac{f}{10^6}\right)\cdot\left(1 + j\cdot\frac{f}{10^7}\right)}$$

$$Angle\_Av(f) := -atan\left(\frac{f}{10^5}\right) - atan\left(\frac{f}{10^6}\right) - atan\left(\frac{f}{10^7}\right)$$

Setting this expression equal to -135 degrees = -3π/4 radians, and solving for f

$$f = 1.000\cdot MHz$$

At this frequency, the magnitude of the open loop gain is

$$Mag\_Av(f) := \frac{\left(10^5\right)}{\left[1. + \left(\frac{f}{10^5}\right)^2\right]^{\frac{1}{2}}\cdot\left[1. + \left(\frac{f}{10^6}\right)^2\right]^{\frac{1}{2}}\cdot\left[1. + \left(\frac{f}{10^7}\right)^2\right]^{\frac{1}{2}}}$$

At the -135 degree frequency, 1.00 MHz, the magnitude of the open-loop voltage gain is

$$Mag\_Av\left(1\cdot10^6\right) = 7.001 \times 10^3$$

In decibels,

$$Mag\_Av\_dB := 20\cdot\log\left(7\cdot10^3\right) \qquad Mag\_Av\_dB = 76.902 \times 10^0$$

Thus the true results a quite close to the graphically predicted results.

If strapped for a gain that is considerably less than 77 dB, the amplifier will oscillate at the frequency where the phase shift passes through -180 degrees, this is found by setting the above expression for the phase angle of Av(jf) to -π radians:

$$-\pi = -atan\left[\frac{f}{\left(1.0 \times 10^5\right)}\right] - atan\left(\frac{f}{1.0 \times 10^6}\right) - atan\left(\frac{f}{1.0 \times 10^7}\right)$$

$$f := 3.331\cdot MHz$$

Ex #3. To make the op amp *unconditionally stable*, no matter what closed-loop voltage gain it is strapped for, we consider the worst-case situation where the closed loop gain is unity, so the open loop gain is the same as the loop gain. We desire to increase capacitance C1 such that the first break frequency f_1 is lowered so that the magnitude of the open-loop voltage gain at the -135 degree phase shift frequency (f_2) is unity.

To calculate this value, replace f_1 by f_{1new} in the open-loop gain magnitude expression above. Then, evaluate it at $f = f_2 = 10^6$ Hz. Finally, set this expression equal to unity and solve for the resulting value of f_{1new}.

$$1 = \frac{\left(10^5\right)}{\left[1. + \left(\frac{10^6}{f_{1new}}\right)^2\right]^{\frac{1}{2}} \cdot \left[1. + \left(\frac{10^6}{10^6}\right)^2\right]^{\frac{1}{2}} \cdot \left[1. + \left(\frac{10^6}{10^7}\right)^2\right]^{\frac{1}{2}}}$$

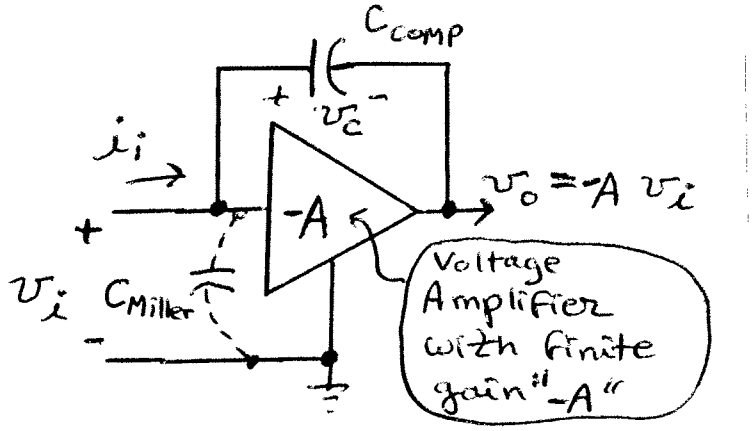
$$f_{1new} := 14.21 \cdot Hz$$

If Rth1 is 10 kΩ, then the value of C_1 required to lower the first break frequency to $f_{1new} = 14.21$ Hz is

$$C_1 := \frac{1}{2 \cdot \pi \cdot 10 \cdot k\Omega \cdot 14.21 \cdot Hz} \qquad C_1 = 1.12 \times 10^{-6} F$$

This is a very large value of capacitance, which would be fairly expensive, and would take up a lot of space on a circuit board.

In order to dramatically reduce the size of the compensating capacitor, the concept of "Miller capacitance multiplication" is used. Instead of connecting the compensating capacitor between the output node of the differential amplfier stage and ground (where the original parasitic capacitance C1 is located), the compensation capacitor is placed across the output and input terminals of the preamplifier stage exhibiting finite voltage gain "-A" as shown in the diagram below:



The voltage across the compensating capacitor, vc(t), is

$$vc(t) = \frac{1}{Ccomp} \cdot \int_{-\infty}^{t} i_1 \, dt$$

But the voltage across the capacitor vc(t) may be expressed in terms of vi(t) since voltage vi(t) appears on the left terminal of Ccomp and voltage Avi(t) appears on the right terminal of the capacitor.

$$vc(t) = vi(t) - (-A \cdot vi(t)) = (1 + A) \cdot vi(t)$$

Thus

$$(1 + A) \cdot vi(t) = \frac{1}{Ccomp} \cdot \int_{-\infty}^{t} i_1 \, dt$$

$$vi(t) = \frac{1}{(1 + A)Ccomp} \cdot \int_{-\infty}^{t} i_1 \, dt = \frac{1}{C_{Miller}} \cdot \int_{-\infty}^{t} i_1 \, dt$$

Thus looking betwem the input terminal of the amplifier and ground we have an equivalent capacitance (Miller capacitance) $C_{Miller} = (1+A)*Ccomp$.

Assuming that the second stage of the op amp (the inverting voltage preamplifier stage) has a voltage gain of -A = -5000, then for $C_{Miller} = 1.12$ μF, we require

$$Ccomp = \frac{C_{Miller}}{1 + A}$$

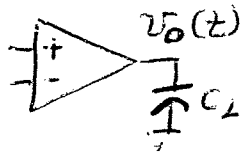
$$Ccomp := \frac{1.12 \cdot \mu F}{1 + 5000} \qquad Ccomp = 223.955 \times 10^{-12} F$$

Thus Ccomp need only be 224 pF, which does not take up much space on the circuit board, nor costs very much!

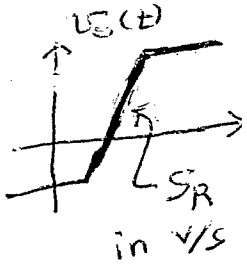
Op Amp Slew Rate "S_R" Specification

We define the slew rate of an OP AMP as the maximum possible rate of change of the OP AMP's output voltage:

$$S_R = \left(\frac{d}{dt}v_0(t)\right)_{Max}$$



The slew rate of an OP AMP is limited because its output current sourcing/sinking capability is "current-limited" to |Iout| < Imax. (For example, for a 741 OP AMP, Imax is limited to 5 mA. For a 411 OP AMP, Imax is limited to 20 mA.)



As the OP AMP's input changes abruptly, the OP AMP's output voltage can only change as fast as its output capacitance (C_L) can be charged, which is limited to Imax Coulombs per second. This maximum rate of change if vo(t) is called the OP AMP's slew rate, where

$$I_{MAX} = C_L \cdot \frac{d}{dt}v_0(t)$$

Thus

$$S_R = \left(\frac{d}{dt}v_0(t)\right)_{Max} = \frac{I_{MAX}}{C_L}$$

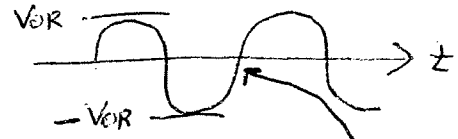
A typical slew rate is 0.6 V/μs for a 741 OP AMP and 15 V/μs for a 411 OP AMP.

Full Power Frequency Response

While the "small-signal" frequency response of an OP AMP circuit is limited by OP AMP's bandwidth (BW), the "large-signal" response is often limited even further by the slew rate specification of the OP AMP.

Consider a sinusoidal OP AMP output voltage given by

$$vo(t) = V_{OR} \cdot \sin\left(2 \cdot \pi \cdot f_p \cdot t\right)$$



Where "V_{OR}" is the maximum rated output voltage, which is usually the full allowable output voltage "swing" usually about 10 V.

And where "fp" is the "full-power response" break frequency, above which vo(t) is no longer able change fast enought to remain sinusoidal.

Maximum Rate of change $= V_{OR} 2\pi f_p$

Taking the derivative of the above expression for vo(t) w.r.t. time yields:

$$\frac{d}{dt} vo(t) = V_{OR} \cdot 2 \cdot \pi \cdot f_p \cdot \cos\left(2 \cdot \pi \cdot f_p \cdot t\right)$$

Note that $V_{OR} \cdot 2 \cdot \pi \cdot f_p$ is the maximum value of dvo(t)/dt

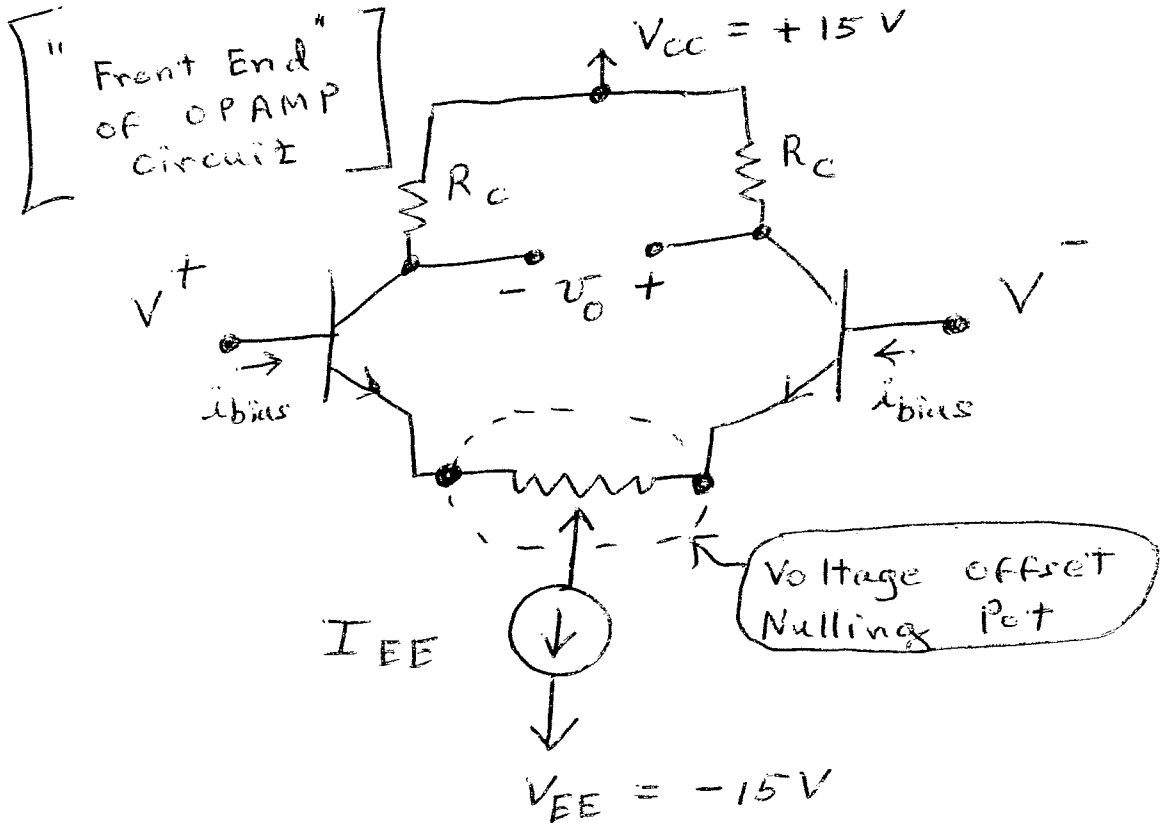
Thus, $$S_R = \left(\frac{d}{dt} v_0(t)\right)_{Max} = V_{OR} \cdot 2 \cdot \pi \cdot f_p$$

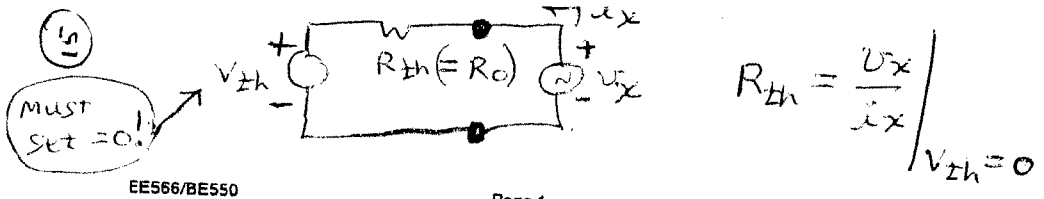
Thus $$f_p = \frac{S_R}{2 \cdot \pi \cdot V_{OR}}$$

OP AMP Offset Voltage Nulling

Due to mismatches in the transistors in the differential pair at input of OP AMP, I_{EE} does not divide equally even when Vplus = Vminus. Thus the output voltage of the differential amplifier, Vo, might differ from zero by as much as 3 mV. As the differential pair changes temperature, there may be an offset voltage drift on the order of 0.1 μV/degree C.

In applications where such an offset voltage is undesired, an offset voltage nulling pot may be added to the circuit, as shown below. It allows mismatches in the transistors to be evened out, so that I_{EE} divides equally between the two transistors when Vplus = Vminus.



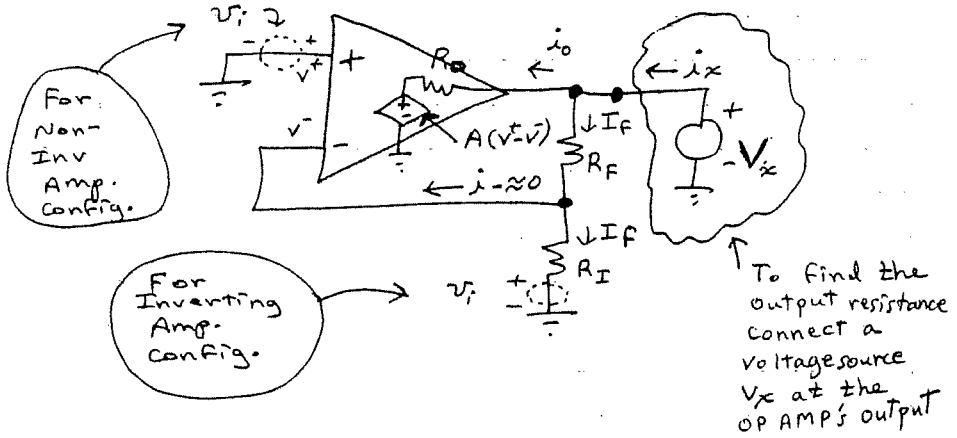


OUTPUT IMPEDANCE OF OPERATIONAL AMPLIFIER CIRCUITS WITH NEGATIVE FEEDBACK

To find the output impedance of an OP AMP circuit, we employ linear superposition by reducing the input voltage (Vi) to zero. Then both the inverting and non-inverting OP AMP circuit configurations become the same, as shown in the circuit below. Next we connect a voltage source (Vx) between the circuit's output terminal and ground, and then we determine the current (Ix) that flows through source Vx into the output terminal. Then the equivalent output resistance of the circuit, Rout, is given by

$$Rout = \left.\frac{Vx}{Ix}\right|_{v_i = 0} \qquad (1)$$

Circuit used to Calculate Output Impedance of OP AMP with Negative Feedback



Note: by setting $v_i = 0 \Rightarrow V_{th} = 0$

Analysis holds for both the inverting and non-inverting OP AMP Configurations.

Using KCL at the output node,

$$Ix = Io + If \qquad (2)$$

But Io can be calculated in terms of Vx:

$$Io = \frac{Vx - A\cdot(Vplus - Vminus)}{Ro} \qquad (3)$$

Where $Vplus = 0$ (This pin is grounded)

And $Vminus = \frac{Ri}{Ri + Rf}\cdot Vx$

Making these substitutions, (3) becomes

$$Io = \frac{Vx - A\cdot\left(0 - \frac{Ri}{Ri + Rf}\cdot Vx\right)}{Ro} \qquad (4)$$

Simplifiying (4) yields

$$Io = Vx\cdot\frac{(Ri + Rf + A\cdot Ri)}{((Ri + Rf)\cdot Ro)} \qquad (5)$$

If can be calculated from Vx,

$$If = \frac{Vx}{Rf + Ri} \qquad (6)$$

Substituting (5) and (6) into (2) yields

$$Ix = Vx \cdot \frac{(Ri + Rf + A \cdot Ri + Ro)}{((Ri + Rf) \cdot Ro)} \qquad (7)$$

The OP AMP circuit's output impedance is

$$Rout = \frac{Vx}{Ix}\bigg|_{Vi=0} = \frac{Ro}{1 + \frac{1}{(Ri + Rf)} \cdot A \cdot Ri + \frac{Ro}{(Ri + Rf)}}$$

Let the voltage division ratio of the external negative feedback resistor network be defined as the "return ratio" β

$$\beta = \frac{Ri}{Ri + Rf} \qquad \text{Then} \qquad Rout = \frac{Ro}{1 + A \cdot \beta + \frac{Ro}{Ri + Rf}} \qquad (8)$$

Assuming that Ro is much less than (Ri+Rf), (8) simplifies to

$$Rout = \frac{Ro}{1 + A \cdot \beta} \qquad (9)$$

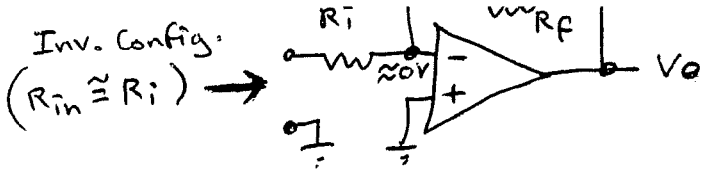
Thus the output resistance of the op amp strapped with negative feedback is EVEN LOWER THAN the output resistance of the open-loop OP AMP (Ro), which is already quite low! The output resistance of the overall circuit is approximately Ro divided by the magnitude of the loop gain, $A\beta$ (for large loop gains).

As an example, consider an inverting amplifier made with an op amp whose output resistance Ro = 25 ohms, open loop gain A = 10^5, and strapped for a gain of 100 (β = 0.01). Then

$$Rout = \frac{25}{1 + 0.01 \cdot 10^5} \qquad Rout = 0.025 \text{ Ohms}$$

But remember that the op amp is current limited to about 25 mA!

BUT REMEMBER THAT THE OP AMP IS INTERNALLY CURRENT-LIMITED TO ABOUT + OR - 25 MA, THEREFORE SMALL LOAD RESISTANCES (LESS THAN ABOUT 10V/25MA = 400 Ω CANNOT BE DRIVEN!



Input Impedance of Non-inverting OP AMP Configuration (Voltage Follower with Gain)

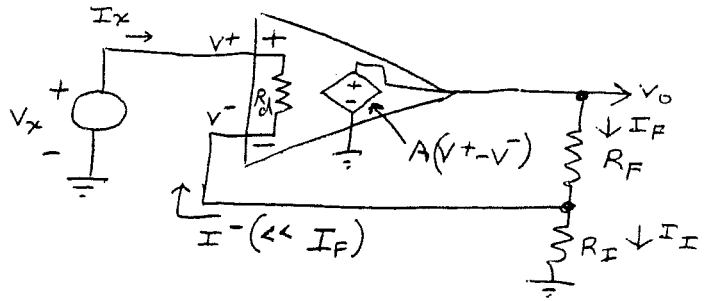
While the inverting op-amp amplifier circuit has an input impedance that is approximately equal to the value of input resistor Ri (since virtual ground exists on the other side of Ri), the input resistance of the non-inverting configuration is not so obvious.

Because the (+) input connects to virtual ground through the internal differential input resistance of the op amp, Rd, it might appear that the input resistance of this configuration is Rd. However, it will be shown below that the actual input resistance is much greater than this, due to the fact that the voltage across Rd is amplified and fed back to the (-) input.

As shown below, imagine that a voltage source (Vx) is applied between the input terminal and ground, and the current through this source is Ix, then the input resistance of the amplifying circuit is

$$Rin = \frac{Vx}{Ix} \qquad (10)$$

CIRCUIT USED TO FIND THE INPUT IMPEDANCE OF A NON-INVERTING OP AMP AMPLIFIER CIRCUIT



Ix can be calculated in terms of Vx and Vminus:

$$Ix = \frac{Vx - Vminus}{Rd} \qquad (11)$$

If we assume that Iminus is neglibigle compared to If, then If = Ii, and we can use the voltage divider equation to find the approximate value of Vminus:

$$Vminus \approx \frac{Ri}{Rf + Ri} \cdot Vo \qquad (12)$$

Furthermore, Vo can be found in terms of Vx (= Vplus) and Vminus.

$$Vo = A \cdot (Vplus - Vminus) = A \cdot (Vx - Vminus) \qquad (13)$$

Substituting (13) into (12) yields

$$Vminus = \frac{Ri}{(Rf + Ri)} \cdot A \cdot (Vx - Vminus) \qquad (14)$$

Solving (14) for Vminus yields

$$Vminus = Vx \cdot Ri \cdot \frac{A}{(Rf + Ri + Ri \cdot A)} = \frac{A \cdot \frac{Ri}{Rf + Ri}}{1 + \frac{Ri}{Rf + Ri} \cdot A} \cdot Vx \qquad (15)$$

Using the definition of "RETURN RATIO", the voltage attenuation of the external resistive feedback network, β

$$Vminus = \frac{A \cdot \beta}{1 + \beta \cdot A} \cdot Vx \quad \text{Where} \quad \beta = \frac{Ri}{Rf + Ri} \qquad (16)$$

Substituting this result into (11)

$$Ix = \frac{\left[Vx - A \cdot \frac{\beta}{(1 + A \cdot \beta)} \cdot Vx \right]}{Rd} \qquad (17)$$

Thus, the desired result is

$$Rin = \frac{Vx}{Ix} = (1 + A \cdot \beta) \cdot Rd \qquad (18)$$

The input resistance of the open-loop OP AMP (Rd), which is already quite large, is effectively multiplied by the magnitude of the loop gain, Ab, (for large loop-gain magnitudes). It is not uncommon for Rd of an OP AMP to be 1 Megohm. Thus, for a follower strapped for a closed-loop voltage gain of 101 (β = 0.01) and an open loop gain A = 10^5, then

$$Rin = (1 + A \cdot \beta) \cdot Rd = \left(1 + 10^5 \cdot 0.01\right) \cdot 10^6$$

$$Rin = 1.01 \cdot 10^9 \quad = 1 \text{ Gigohm!}$$

However, ***in a real circuit, the input resistance will most certainly be considerably lower than this, since the shunting resistance of the package and the circuit board insulation will be lower than 1 Gigohm!***

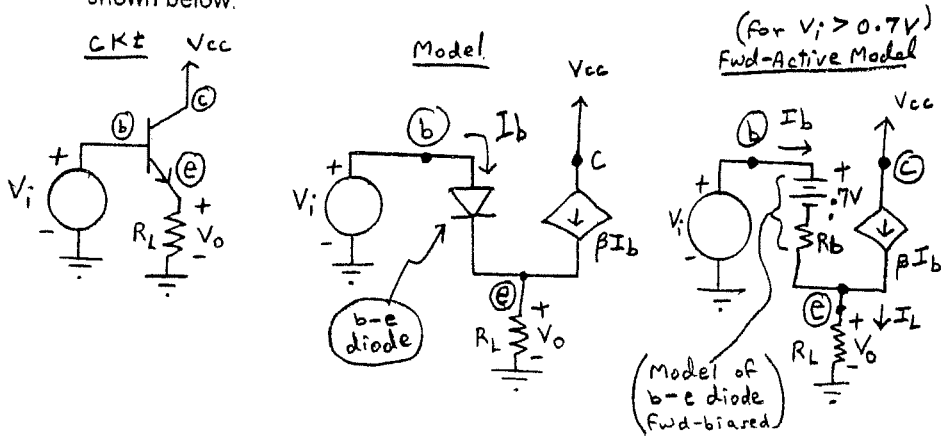
POWER OPERATIONAL AMPLIFIERS

Recall that the typical OP AMP is current-limited to about + or - 25 mA. This implies that, even though the output resistance of an OP AMP amplifier circuit with negative feedback is very low, low load resistances still cannot be driven, due to the OP AMP's output current limiting circuitry, which protects the OP AMP from burning out, since large currents would require large quantities of heat to be dissipated inside the OP AMP.

This output current limitation can be overcome by adding an external complementary symmetry output current booster circuit, which is formed using two resistors, two diodes, and an npn and a pnp power transistor (both are mounted on "heatsinks"). The BJTs are both connected in an "emitter follower" configuration to drive even a relatively low-valued load resistance RL to the op amp output voltage.

This operation of this circuit is based upon the fact that the output voltage of an emitter follower stage follows the input voltage (minus the 0.7 V b-e junction drop), but it has a high input impedance (about β*RL), and a low output impedance (about Rb/β) where β is the forward-current transfer ratio parameter of the transistor, with a typical value of 250.

First, we shall review the operation of the basic npn BJT emitter follower amplifier stage whose circuit and equivalent circuit model are shown below:



I. Analysis of BJT Emitter Follower Stage

Part 1. Finding the Output Voltage of an Emitter Follower, Vo

$$Ib = \frac{Vi - 0.7 - Vo}{Ri} \qquad (1)$$

$$IL = Ib(1 + \beta) \qquad (2)$$

$$Vo = RL \cdot IL \qquad (3)$$

Substituting (1) and (2) into (3) yields

$$Vo = RL \cdot \frac{Vi - 0.7 - Vo}{Ri} \cdot (1 + \beta) \qquad (4)$$

Solving (4) for Vo yields

$$Vo = RL \cdot \frac{(Vi \cdot (\beta + 1)) - .7 \cdot (\beta + 1)}{(Ri + RL \cdot (\beta + 1))} \qquad (5)$$

As long as **Ri << RL(β+1)**, which is usually true since β is large, Ri can be ignored, and then (5) dramatically reduces to

$$Vo = Vi - 0.7 \qquad (6)$$

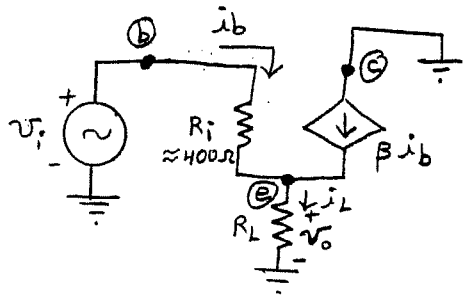
Thus the output voltage "follows" the input voltage (minus the 0.7 V b-e junction drop).

The ac voltage gain is 1, therefore what use is this circuit? The answer lies in its low output resistance, Rin, and high input resistance Rout.

Part 2. Finding the Input Resistance of an Emitter Follower Stage

Because the input resistance Rin is an "ac" parameter defined as "the *change* in Vin divided by the *change* in Ib", we must use the principle of superposition to construct the "ac small-signal" circuit model shown below, which requires that the 0.7 V dc source in the above circuit model to be reduced to zero. The lowercase symbols ib(t) and vo(t) represent only the time-varying "ac" components of the base current and output voltage, with the constant "dc" components of Ib and Vo ignored.

AC Small-Signal Model of Emitter Follower Ckt



Thus the input resistance is the ratio of the changing (ac) part of the input voltage Vi, vi, to the changing (ac) part of the input current Ib, ib.

$$Rin = \frac{vi}{ib} \tag{7}$$

Working as before, we see that

$$ib = \frac{vi - vo}{Ri} \tag{8}$$

and

$$vo = RL \cdot ib \cdot (\beta + 1) \tag{9}$$

Substituting (8) into (9) yields

$$vo = RL \cdot \frac{(vi - vo)}{Ri} \cdot (\beta + 1) \tag{10}$$

Solving for vo yields

$$vo = RL \cdot vi \cdot \frac{(\beta + 1)}{(Ri + RL \cdot (\beta + 1))} \tag{11}$$

Substituting (11) into (8) yields

$$ib = \frac{vi - RL \cdot vi \cdot \dfrac{(\beta + 1)}{(Ri + RL \cdot (\beta + 1))}}{Ri}$$

Solving for vi,

$$vi = ib \cdot (Ri + RL \cdot (\beta + 1)) \tag{12}$$

Thus

$$Rin = \frac{vi}{ib} = Ri + RL \cdot (\beta + 1) \tag{13}$$

If we make the same assumption as before, Ri << RL(β+1), we find that the input resistance of the emitter follower stage is approximately given by

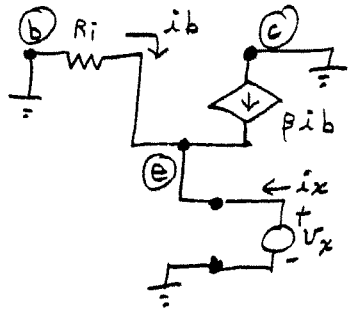
$$Rin = RL \cdot (\beta + 1) \tag{14}$$

Since β is large, this input impedance is usually very high.

Part 3. Finding the Output Resistance of an Emitter Follower Stage

To find the equivalent output resistance looking back from the output terminals where RL has been connected, we may set the input signal source vi to 0, and replace RL by a voltage source, vx that passes source current ix. This circuit is shown in the space below.

Circuit for Deriving the Equivalent Output Resistance of an Emitter-Follower Amplifier



Then the equivalent output resistance, Rout, is given by

$$\text{Rout} = \frac{vx}{ix} \qquad (15)$$

KVL applied around the input loop =>

$$ib = \frac{0 - vx}{Ri} \qquad (16)$$

KCL applied at the emitter node =>

$$ix = -(\beta + 1) \cdot ib \qquad (17)$$

Substituting (16) into (17) yields

$$ix = -(\beta + 1) \cdot \frac{0 - vx}{Ri} \qquad (18)$$

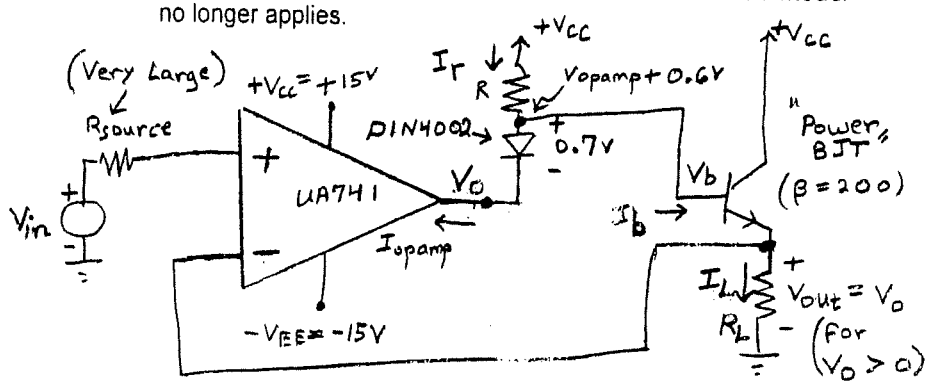
Thus

$$\text{Rout} = \frac{vx}{ix} = \frac{Ri}{\beta + 1} \qquad (19)$$

Since β is large, this output impedance is usually quite low.

II. Use of an npn Emitter Follower to Connect a Current-limited OP AMP to a High-current Load

The OP AMP in the circuit below is connected to an external npn emitter-follower output stage. This circuit contains a 0.7 V diode level-shifting circuit that uses a forward-biased diode to cancel out the BJT's 0.7 V b-e internal junction drop. Thus Vout = Vo, assuming that Vcc > Vo, and Vo is kept positive. If Vo goes negative, the npn BJT b-e junction becomes reverse biased, and the BJT enters "cut-off", where the controlled source BJT model no longer applies.



There are two considerations that influence the choice of bias resistor R. These are best illustrated by an example. Imagine that RL = 8 ohms, which must be driven to values between 0 and 10V. Then Vcc must be comfortably greater than the top end of this range, say Vcc = 15 V. The power transistor has a β of 200. The OP AMP is current-limited to + or - 25 mA.

Consideration 1: Consider the case when the OP AMP is driven to the top end of its range,

$$Vo = 10 \text{ V} \quad RL = 8 \text{ Ohms} \quad IL = \frac{Vo}{RL} \quad Vcc = 15 \text{ V}$$

$$\text{Then } Vb = Vo + 0.7 \quad Vb = 10.7 \text{ V}$$

And

$$Ir = \frac{Vcc - Vb}{R} > Ib = \frac{IL}{(\beta + 1)} \qquad \beta = 200$$

So that some residual current is available to flow through the diode to keep it forward biased, thus Iopamp is very small.

$$Rmax = \frac{(Vcc \cdot \beta + Vcc - Vb \cdot \beta - Vb)}{IL}$$

$$Rmax = 691.44 \text{ Ohms}$$

Consideration 2

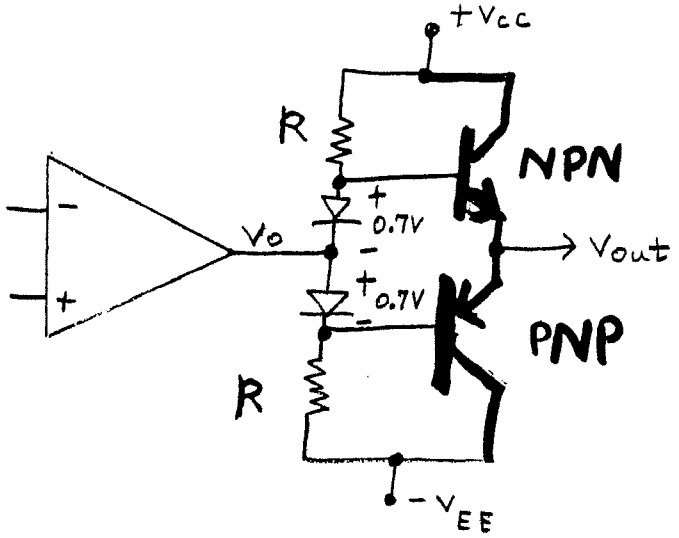
When Vo = 0V, the current Ib = 0, and all of the current through Ir goes through the op amp. Since the op amp is current limited to 25 mA,

$$\frac{Vcc - 0.7}{Rmin} = 0.025 \qquad Rmin = 572 \text{ Ohms}$$

Conclusion: Pick R = 620 ohms

III. The Complementary Symmetry Output Stage

The circuit above only operates for positive values of output voltage. In order to allow both positive and negative values of output voltage, the following "complementary symmetry" circuit (as shown in our textbook) may be used:



When Vi > 0, the npn BJT is forward active, and the pnp BJT is cut off. When Vi < 0, and pnp BJT is forward active, and the npn BJT is cut off.

NOTE: This entire circuit can be thought of as a power OP AMP, so if it were used in a non-inverting or inverting amplifying configuration, the feedback resistor would typically connect to the junction of the two BJT emitters, rather than the OP AMP output.

Example Power OP AMP
National Semiconductor
LM12 — 125 W maximum power dissipation