3.4 The Instrumentation Amplifier (3-op amp differential amplifier)

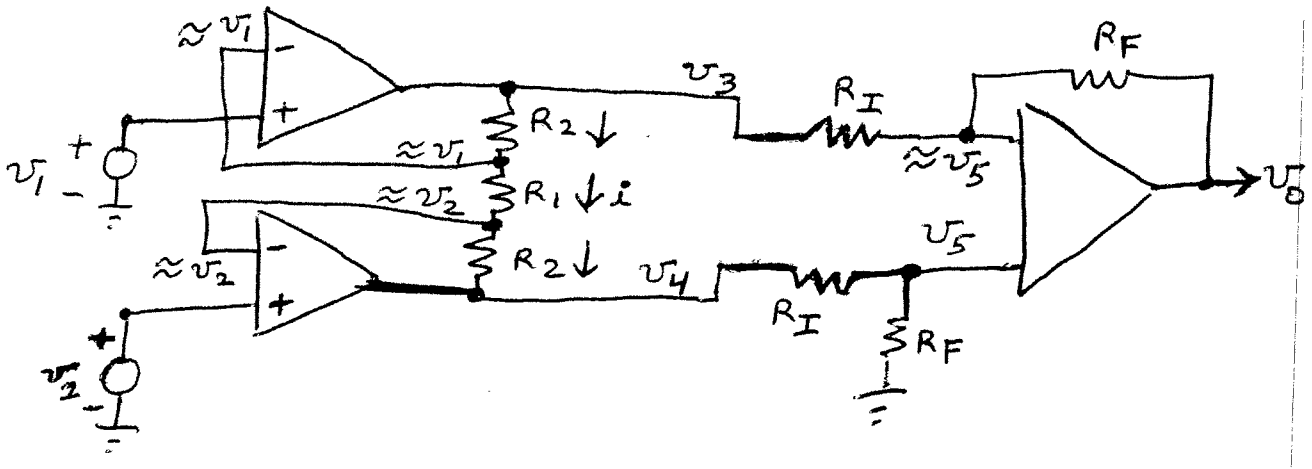
The 1-op amp differential amplifier that was just introduced does not exhibit very high input impedance (Rin = R3 + R4), so it tends to "load down" the available output signal voltage from a high impedance transducer.

In addition, we have just seen that the two Ri's and the two Rf's in the 1-op amp differential amplifier circuit must be *closely matched* in order to keep the common-mode gain low, so that the common-mode rejection ratio (CMRR) will be high, and the amplier will be relatively insensitive to common-mode noise.

It is possible to peform "laser trimming" at the time of manufacture to make the two Ri's and the two Rf's well matched, but that fixes the differential gain of the amplifier. If we desire the gain of the differential amplifier to be adjustable after manufacture, or "field programmable", the user will have to vary the differential gain by varying the two Ri's (or the two Rf's), and it will be the user's responsibility to keep these two gain-setting resistors (the two Ri's) well-matched, which is hard to do!

The 3-op amp differential amplifier (instrumentation amplifier) shown below solves both of these problems. It exhibits a very high input impedance and it permits the differential gain to be varied by changing just one resistor, instead of two matched resistors!

Instrumentation Amplifier Circuit



Consider the 2-op amp input stage on the left

(a) Differential Gain Calculation of 2-op amp input stage

Because negative feedback is clearly present, we may assume the two input op amps are in their linear amplifying region, and so we may use Rule #1 of the ideal op amp (virtual voltage rule) we may calculate the current downward through resistor R1

$$i = \frac{v_1 - v_2}{R_1}$$

By Rule #2 of the ideal op amp (zero input current rule), this current "i" must also flow through each of the R2 resistors, and thus

$$v3 - v4 = i\left(R_2 + R_1 + R_2\right) = \frac{v_1 - v_2}{R_1}\cdot\left(2\cdot R_2 + R_1\right)$$

The differential voltage gain provided by this stage (which has both differential inputs AND differential outputs) is therefore given by

$$\frac{v_3 - v_4}{v_1 - v_2} = \frac{2\cdot R_2 + R_1}{R_1}$$

(b) Common-mode Gain (let Vcm = v2 = v1)

$$i = \frac{Vcm - Vcm}{R_1} = 0$$

Therefore there is no voltage drop across R1 or either of the R2's, and

$$v_3 = v_4 = V_{cm}$$

Therefore the common-mode gain of this 2-op amp input stage is

$$Av_{cm} = \frac{v_3}{v_{cm}} = \frac{v_4}{v_{cm}} = 1 \qquad CMRR = \frac{Av_{diff}}{Av_{cm}} = Av_{diff}$$

Note that the use of the 2-op amp input stage shown below is clearly superior to using two separate non-inverting voltage amplifier stages each with a voltage gain equal to Av = (2R2+R1)/R1, since the common-mode signal would be amplified along with the differential mode signal, thereby increasing the overall common-mode gain of the overall 3-op amp instrumentation amplifier.

(c) Connecting the 2-op amp input stage to the 1-op amp differential amplifier stage

The overall differential voltage gain is the product of the differential gains of the input stage and the output stage

$$Av_{diff\_overall} = \left(\frac{2 \cdot R_2 + R_1}{R_1}\right) \cdot \left(\frac{R_F}{R_I}\right)$$

Note that the input impedance of the instrumentation amplifier is nearly infinite, and the differential voltage gain is adjustable by just one resistor, R1!

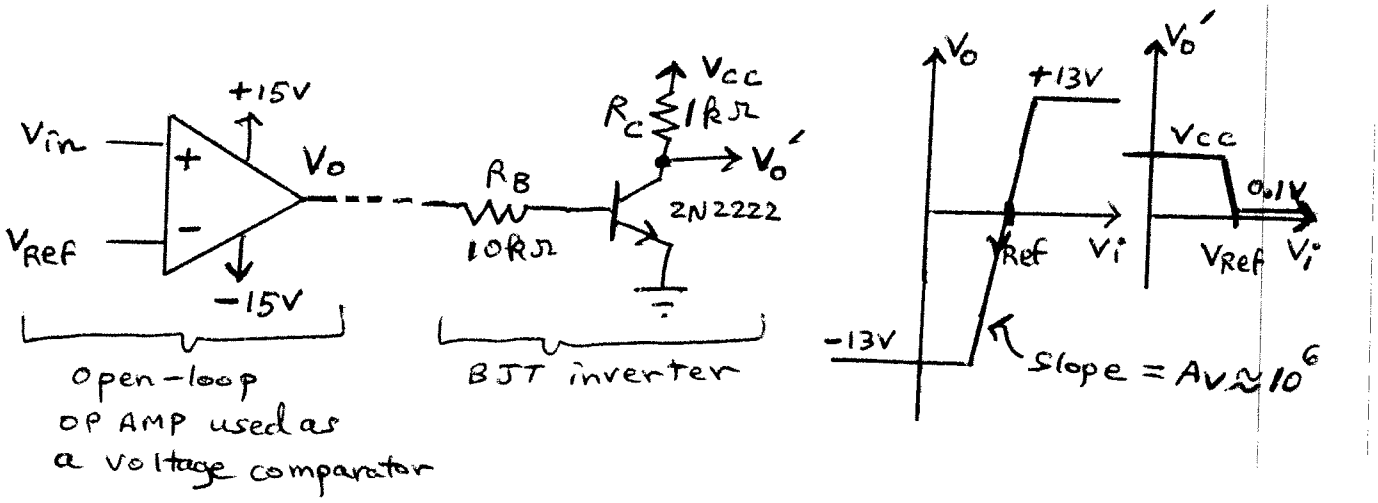
Likewise, the overall common-mode voltage gain is the product of the common-mode gains of the input and output stages

$$Av_{cm\_overall} = Av_{cm\_input\_stage} \cdot Av_{output\_stage}$$

$$Av_{cm\_overall} = 1 \cdot Av_{output\_stage}$$ (nearly zero, depending upon how well matched R_I and R_F are.)

3.5 Op Amp used as Voltage Comparator (1-bit A/D Converter)

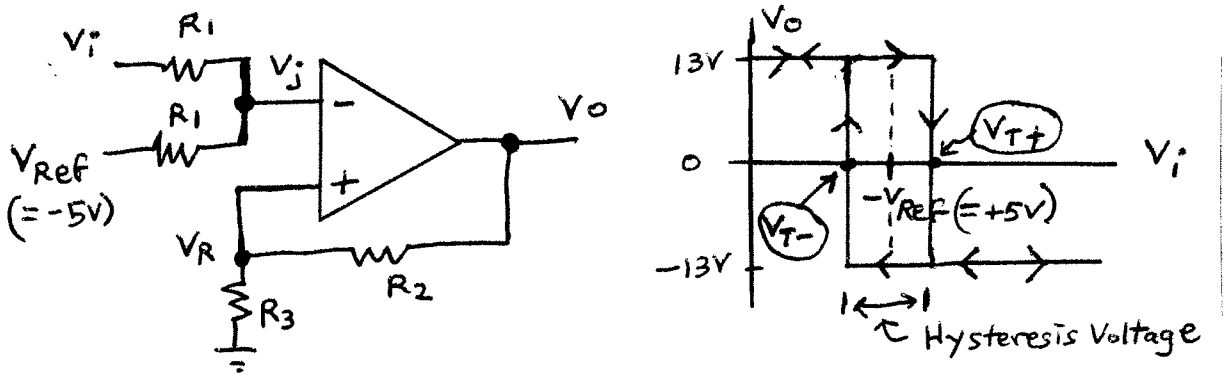
(a) An op amp operated open-loop (with an open-loop voltage gain of 10^6) will function as a voltage comparator, as shown below. It will deliver an output voltage Vo = +13 V when Vin > Vref + $13/10^6$, and will deliver an output voltage that is Vo = -13 V when Vin < Vref - $13/10^6$. There is only a very narrow window of input voltages in the vicinity of Vref for which the output voltage will be in between +13 V and -13 V.



If we desire to convert Vo into a digital logic voltage level that varies between 0 V and Vcc volts, that is more suitable as an input to a microcontroller or digital logic system, then we may connect the output of the operational amplifier to the input of a BJT inverter, as shown above. The resulting inverter's output voltage Vo' is about 0 V (Vcesat) when Vo = 13 V, and hence when Vin > Vref; and Vo' = Vcc (typically Vcc = 5 V) when Vo = -13 V, and hence when Vin > Vref. Note that the sense of the voltage comparison has been inverted as well as level-shifted.

(b) Adding Hysteresis (Schmitt Trigger)

Consider the circuit below:



By linear superposition, the voltage at the (-) input of the op amp, Vj, is

$$V_j = V_i \cdot \left(\frac{R_1}{R_1 + R_1} \right) + V_{Ref} \cdot \left(\frac{R_1}{R_1 + R_1} \right) = \left(\frac{V_i + V_{Ref}}{2} \right)$$

The voltage at the (+) input of the op amp, V_R, is

$$V_R = Vo \cdot \frac{R3}{R2 + R3}$$

Note that there can be two possible values of V_R, since Vo can either be +13 V or -13 V, depending upon whether Vj is less than or greater than V_R, respectively.

To find the input voltage when Vo changes (the comparator "flips") set $V_j = V_R$.

$$\frac{V_i + V_{Ref}}{2} = Vo \cdot \frac{R3}{R2 + R3}$$

Let us assume that we are starting at a sufficiently low level of Vi so that Vj is below V_R and so Vo = +13 V. Then as Vi is allowed to rise, it eventually reaches the point Vi = Vtplus, where the comparator flips (Vj = V_R), and the output changes from +13 V to -13 V, as shown in the Vo vs. Vi voltage transfer curve above.

$$\frac{Vi + V_{Ref}}{2} = (13)\cdot\frac{R3}{R2 + R3}$$

$$Vi = Vtplus = -V_{Ref} + 2(13)\cdot\frac{R3}{R2 + R3}$$

Then as Vi is allowed to fall, Vo changes from -13 V back to +13 V at the input voltage value Vi = Vtminus, which is considerably lower than Vtplus. We may find the value of Vtminus by setting V_R = Vj.

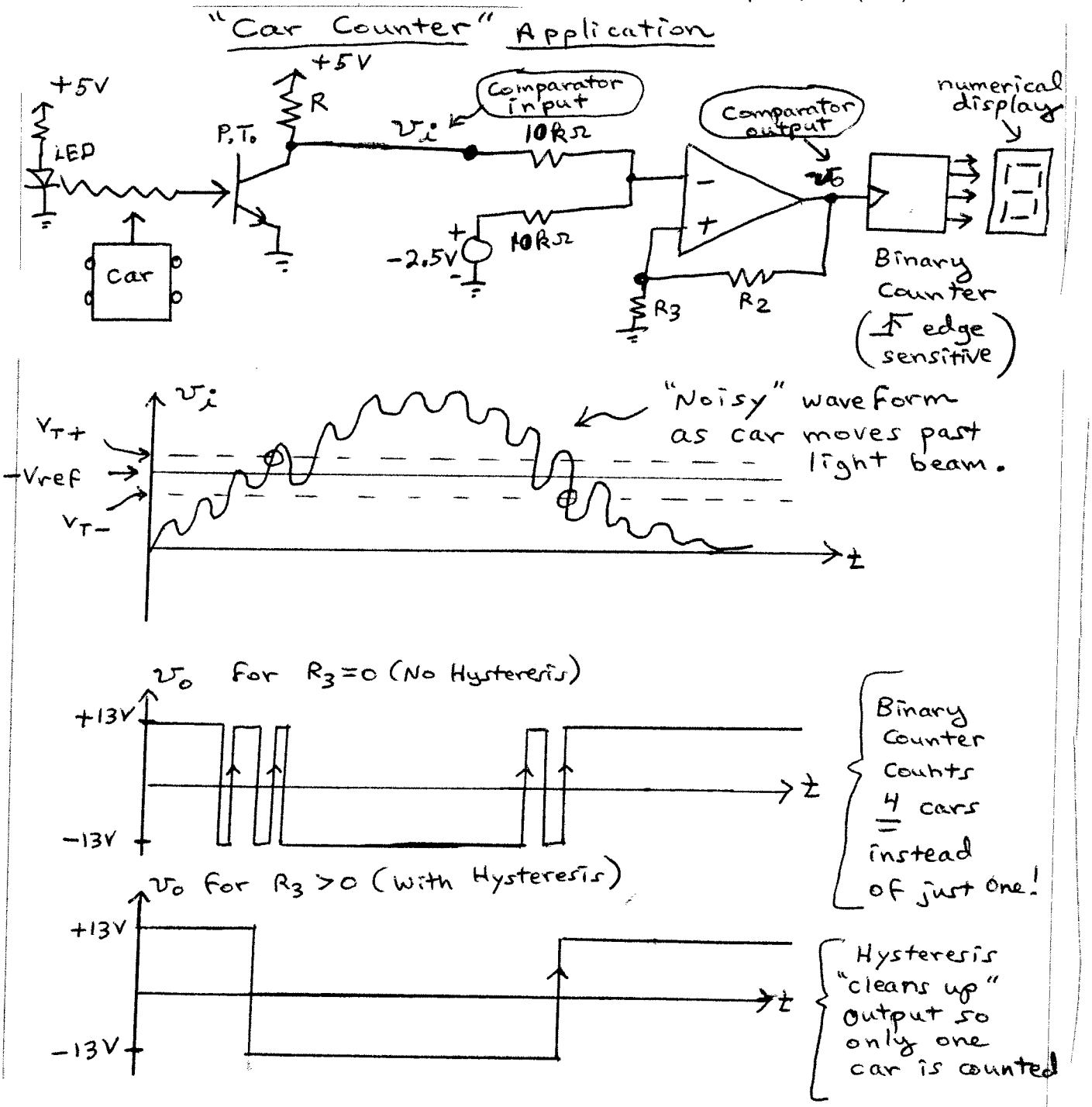
$$\frac{Vi + V_{Ref}}{2} = (-13)\cdot\frac{R3}{R2 + R3}$$

$$Vi = Vtminus = -V_{Ref} - 2\cdot(13)\cdot\frac{R3}{R2 + R3}$$

Note that if R3 = 0, the op amp's (+) input is connected to ground, and there is no hysteresis. The comparator has a single transition point at Vi = $-V_{Ref}$.

Usefulness of Hysteresis

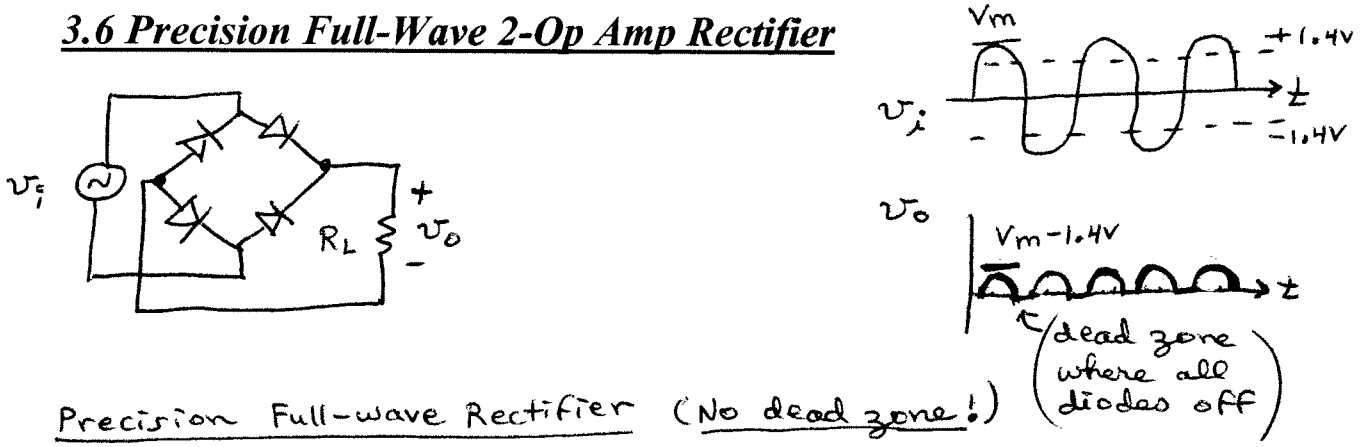
Consider an optical "car counting" application, where cars are counted as they drive past a light beam. As a car begins to block the light arriving at the phototransistor, the transistor leaves saturation and enters its active region, moving toward cutoff. Consequently, the voltage at the collector of the phototransistor, vi(t), begins to rise. Because the car does not break the light beam cleanly, and also due to other environmental factors such as 60 Hz inteference, vi(t) does NOT rise cleanly, but instead there is noise superimposed on vi(t) as shown in the figure below.



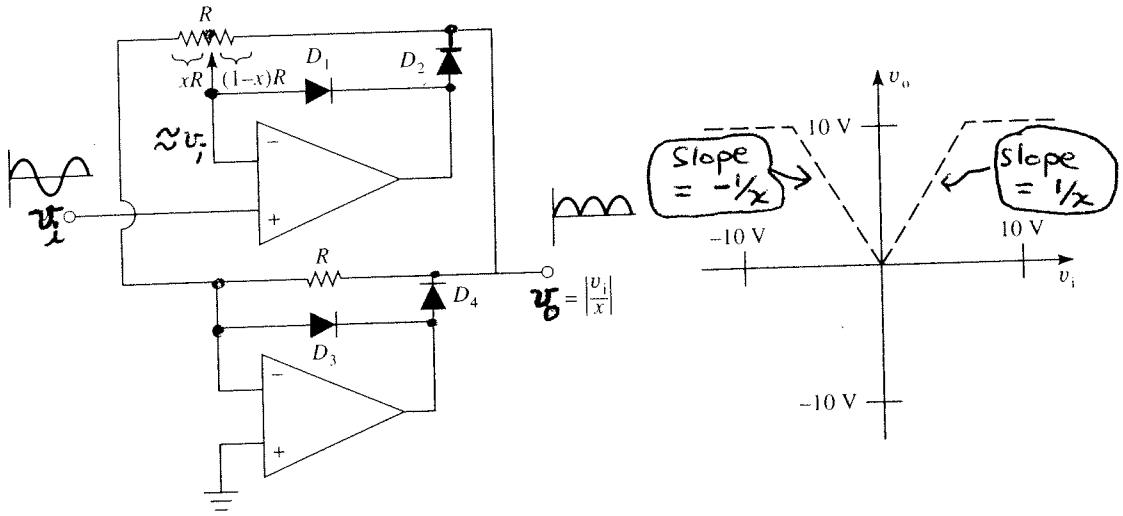
If a comparator without hysteresis (R3 = 0) is used to detect when vi(t) rises and falls past a certain threshold voltage ($-V_{Ref} = 2.5$ V), when vi(t) approaches this threshold, the noise will take vi(t) back and forth across the threshold, resulting in several quick unwanted transitions at the output of the comparator, vo(t), as shown in the figure below. In the example shown, four cars are counted (since the binary counter counts rising edge transitions) instead of the one car that should have been counted!

If a comparator with hysteresis (R3 > 0) is used to detect when vi(t) rises past the "rising threshold voltage" Vtplus and then later falls past the "falling threshold voltage" Vtminus, just one rising edge per car will occur at vo(t), providing that the peak-to-peak noise voltage amplitude remains less than the hysteresis voltage (Vtplus - Vtminus) = 4(13)(R3/(R3+R2)) .

3.6 Precision Full-Wave 2-Op Amp Rectifier



Precision Full-wave Rectifier (No dead zone!)



For vi > 0, D2 and D3 are ON. D1 and D4 are OFF.

Thus the non-inverting op amp "voltage follower" circuit at the top is connected to the output node (vo) with voltage gain vo/vi = (Rf+Ri)/Ri, where Rf = (1-x)R and Ri = xR. Therefore

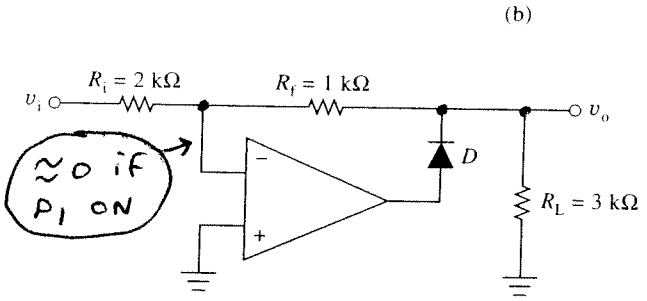
$$\frac{vo}{vi} = \frac{(1-x)\cdot R + x\cdot R}{x\cdot R} = \frac{1}{x}$$

For vi < 0, D1 andD4 conduct D2 and D3 are OFF.

Thus the inverting op amp circuit at the bottom is connected to the output node (vo) with voltage gain vo/vi = -Rf/Ri, where Rf = R and Ri = xR. Thus

$$\frac{vo}{vi} = \frac{-R}{xR} = \frac{-1}{x}$$

Single Op-Amp Full-Wave Rectifier



If Vi > 0, then D1 is OFF, and the OP AMP is disconnected from the circuit

$$Vo = \frac{RL}{Ri + Rf + RL} \cdot Vi = \frac{3}{1 + 2 + 3} \cdot Vi = \frac{Vi}{2}$$

If Vi < 0, then D1 is ON, and the OP AMP is in inverting amplifier configuration

$$Vo = \frac{-Rf}{Ri} \cdot Vi = \frac{-1}{2} \cdot Vi$$

Disadvantages:

a. Input resistance changes as vi crosses zero.
b. Output resistance changes as vi crosses zero.
c. This circuit cannot rectify high frequency sine waves because OP AMP is driven into saturation during positive half of input cycle and it takes time for the OP AMP to come out of saturation after vi drops below zero.