Discrete BJT Amplifier Project

(A) Shunt FB Amplifier
(B) Complementary Pair Amplifier
C) Shunt-Series FB Pair Amplifier
(D) Series-Shunt FB Pair Amplifier
(E) Cascode Amplifier
F) Differential Amplifier
G) Emitter Follower

The several discrete BJT amplifier circuits cited above are illustrated below, with abbreviated design notes provided for each circuit. There will be a limited opportunity for clarifications in response to questions raised in a class. In general you are encouraged to use other references, and are free to consult with others. However material copied from other sources and included in the report must be attributed appropriately. Acknowledgement of particularly noteworthy aid from individuals also is appropriate. One circuit from among those listed will be assigned separately to each of several teams; both team and circuit assignments are made by the instructor by more or less random selection . Each team will make appropriate arrangements among themselves to complete the assignment on time. However individual task assignments must be stated explicitly in the report. More than one person may work on the same task, but one person shall be designated as the principal task leader. Note that while only one report is required from each team, each member of the team is responsible for **all** of the report content.

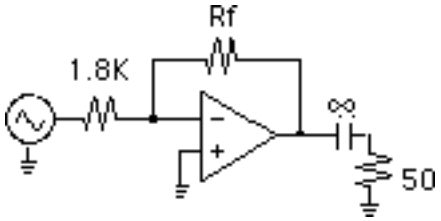
The report format used (described elsewhere) and its technical content shall be at a level commensurate with the prerequisites of ECE 414. Reports are not expected either to be literary masterpieces or works of graphic art. They are however expected to approach adequately the appearance and substance of a professional engineering report. Clarity of presentation, an appropriate technical vocabulary, proper spelling, and attention to grammar and syntax are indispensable. Each of these considerations is included in the evaluation of the report.

In addition to a written report each project team shall organize and be prepared to make a short presentation of their work to the class as a whole (plan for about 15 minutes for presentation plus about 5 minutes for questions). Parenthetically it is worthwhile to emphasize that involvement of an engineer in an audience for a technical presentation is not a passive activity. In various professional and employment activities you will frequently be expected to listen to presentations, understand what is presented, raise questions for clarification, and relay your understanding to others.

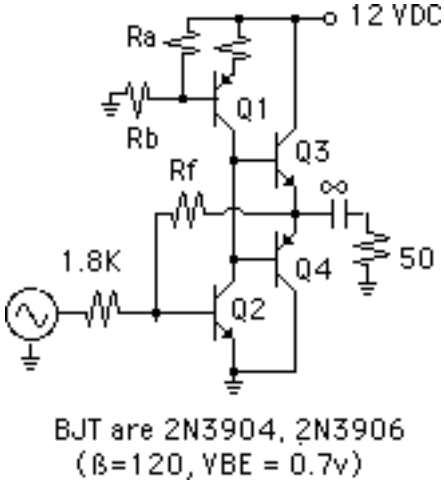
Virtual experiments (i.e. PSpice computations) are to be performed for each circuit as described. The general technical objective is to prepare an informed comparison of estimated circuit performance based on simplified device models with corresponding values computed using the more precise nonlinear mathematical models. In addition there are specific questions posed, for which a response will be expected. Written reports will be evaluated and returned with appropriate comments and suggestions. A digital copy of each team report shall be provided (email or disk) in a timely fashion; the several reports will be consolidated and made available on the course web site.

(A) Shunt FB Amplifier

The amplifier circuit drawn to the right consists of a shunt feedback amplifier (gain) stage driving a Class AB power output stage. The supply voltage is specified at 12v, the source resistance is 1.8 kΩ, and the transistors are assumed to be 2N3904 or 2N3906 respectively. The amplifier is to be capable of providing a 4-volt peak voltage across a 50Ω AC coupled load. The circuit is a discrete implementation of the inverting amplifier configuration drawn below, left.



Note the use of shunt feedback (Rf) to reduce crossover distortion. Rf also provides a means of fixing the Q3-Q4 quiescent emitter voltage.



Q1 operates as a 'current source' to provide the quiescent bias current for Q2 and Q4-Q4.

A number of simplifications can be prearranged to make the design process more tractable. If, for example, the DC (quiescent) current through Rf is made 'large' compared to the Q3 base current the bias current through the 1.8kΩ source resistance is approximately 0.7/1.8 ma; this also is the estimated current through Rf, and this current must be provided by Q3.

The specification calls for providing a 4v peak voltage across 50Ω, corresponding to a peak current of 4/50 = 80 ma. The must be provided from the Q3-Q4 emitters on respective half-cycles, and hence an estimate of the required Q3-Q4 base current can be made. This base current is provided by Q1, which also provides the Q2 quiescent current..

The Q2 collector current is substantially fixed, so that the base current to the Class AB stage varies as the Q3 collector current varies. Maximum base current corresponds to cutting off Q3, and minimum base current corresponds to having all the Q2 current flow through Q3. (These are extreme conditions; for various reasons both extremes distort the output voltage.

You are to design an amplifier to meet the specifications given. Estimate <u>quantitatively</u> the performance expected of the circuit you design, in particular DC bias voltages and currents, and AC gain. Compare your calculated estimates of these quantities against the results of a computer computation using the nonlinear device models. Note that 'comparison' implies an appropriate evaluation also. Use the simplified large-signal and incremental parameter models for calculations.

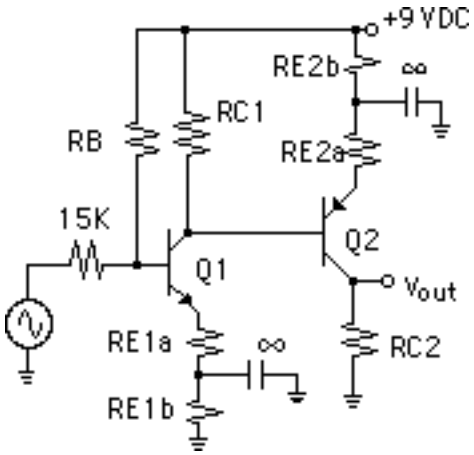
Include <u>explicitly</u> answers to the following questions:
What purpose(s) does Rf serve? How is the DC voltage at the Q4-Q5 emitters determined? How is significant crossover distortion avoided? Include a plot of the emitter currents of both Q4 and Q5 on the same axes, and relate these to a plot of the total load current.

Is Q4 conducting or not in the quiescent state? Is Q5 conducting or not in the quiescent state? If either transistor is conducting estimate the emitter current carried and compare to the computed value.

Comment critically on how you chose the feedback resistor Rf. Respond <u>critically</u> also to the suggestion for obtaining an order of magnitude increase in voltage gain by making a factor of ten increase Rf.

(B) Complementary Pair Amplifier

A two-stage 'Complementary Pair' BJT amplifier circuit diagram is drawn to the right. The ' ∞' symbol is used to indicate that the (unspecified) capacitance is large enough at the (unspecified) signal frequency to have a negligible reactance, i.e. be treated as an AC short-circuit.



The rationale behind a 'complementary pair' cascade is a problem that can arise with a cascade of similar NPN (for example) stages. To avoid saturation the collector voltage of each stage must be greater than the base voltage, enough greater to allow for the collector voltage AC changes. However since the base voltage of the second stage is taken from the collector of the first stage it is inherently larger that the first stage base voltage, and the second stage collector voltage is still higher. But this decreases the amplitude available for the amplified signal. Adding a third stage simply aggravates this condition.

If a PNP second stage is used an increase in PNP base voltage accommodates a desirable higher PNP collector voltage. Moreover a third NPN stage can be cascaded onto the PNP stage without the severe voltage offset problem of a cascade of similar stages.

Estimating the DC bias voltages and currents is simplified considerably under the assumption that the PNP base current is small compared to the NPN collector current. Of course this is not necessarily so but there are two reasons generally favoring such a relationship. Considering the common DC source and the bias configuration one might expect intuitively that the two transistors will have roughly comparable collector currents, and a 2N3906 ß of about 120 then supports the approximation. And a sort of circular reasoning based on an enlightened self-interest suggests that a simplifying approximation relatively easy to implement in fact will be implemented so as actually to simplify the circuit design process. In any event the assumption can be made and subsequently justified explicitly by a verifying the consistency of the assumption with values calculated using it. And of course adjustments can be made if and where needed.

The approximation (recommended) makes the bias calculations for each stage effectively independent of one another. The estimate so made can be refined by a second iteration in which rather than neglecting the PNP base current the value of this current estimated from the first iteration is used. This refinement is rarely if ever necessary.

Design a Complementary Pair amplifier stage using 2N3904 and 2N3906 transistor5s (ß ≈ 120, VBE ≈ 0.7v). Use a supply voltage of 9 volts, and a source resistance of 15kΩ. Estimate the DC bias voltages and currents, and compare these with the results of a computer analysis. Determine the incremental gain for a nominal 1 kHz signal.

The partitioning of the stages for the bias calculation suggests the circuit shown performs as a cascade of two common-emitter stages, each with emitter feedback. Consider the resistors RE1a and RE2a that appear in the emitter paths of the incremental parameter circuit (the other emitter resistors are bypassed). Because of the transistor current amplification this resistance transformed into the transistor base is larger by a factor of ß+1, and this typically is generally significantly larger than rbe with which it is in series. Hence, roughly, an AC voltage v at the base of the NPN device (for example) appears almost entirely across the emitter resistor. The incremental emitter current is essentially equal to the incremental collector current, and the approximate voltage gain for the first stage is –RC1/RE1a. (Note

the 180˚ phase shift) Similarly an estimate for the PNP stage voltage gain is -RC2/RE2a. For the two-stage cascade the gain estimate then is the product. Note however there is also an input transfer loss of RB/(RB + 15k).

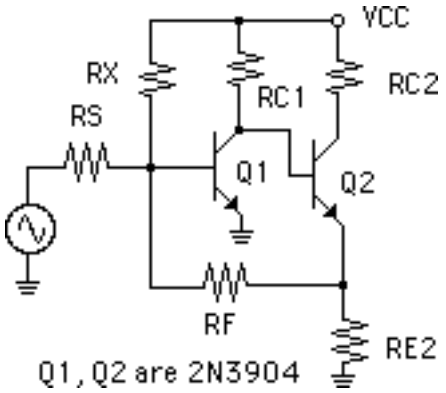
Estimate the DC bias currents and voltages for your design; use the simplified large-signal BJT models. **Be sure** to present explicit justification for each assumption made for your design.

Use the simplified incremental parameter transistor model to estimate the AC voltage gain. Be sure to draw a properly labeled incremental circuit. Compare this estimate against the approximate calculation described above, as well as the computed gain.

In this respect consider further the implication that each stage gain depends largely on the ratio of the collector resistance to the (unbypassed) emitter resistance? Respond critically to the suggestion of obtaining an order of magnitude increase in gain by a factor of ten increase in the collector resistance. Similarly respond critically to the alternative suggestion of obtaining an order of magnitude increase in gain by decreasing the unbypassed emitter resistance by a factor of ten.

C) Shunt-Series FB Pair Amplifier

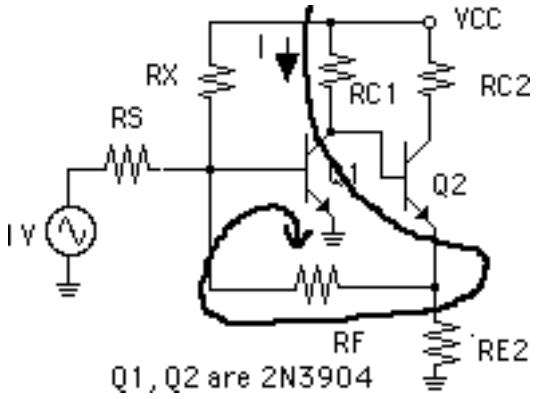
A 'shunt-series feedback pair' DC-coupled amplifier circuit diagram is drawn to the right. The Q2 emitter junction voltage is relatively insensitive to Q2 emitter current changes. Hence the Q2 emitter voltage can be expected largely to track changes in the collector voltage of Q1. In so far as feedback is concerned Q1 should behave essentially the same as if RF is connected directly to the Q1 collector, i.e. as a shunt feedback stage. The stabilized collector voltage of Q1 then serves to support the emitter stabilization of Q2. An advantage of this pairing over cascading disjoint shunt and series feedback stages is the DC coupling, and the consequent improved low-frequency response.



DC analysis of this circuit using the simplified large-signal model of the BJT is straightforward if a bit involved. However for design estimation purposes the DC analysis is simplified considerably if the base current of Q2 can be neglected compared to the collector current of Q1. This is almost certain to be a valid condition in practice because the similar transistors connected in cascade have a common power supply. And as noted elsewhere it is likely to be inherent in the design precisely because of the analytical simplification it provides. In any event, of course, the assumption should be validated by consistency with the consequences of its application. A rarely needed adjustment can be made by redoing the calculation, substituting the Q2 base current calculated with the approximation rather than neglecting it.

The DC coupling to the signal source used in this illustration adds a degree of complication because the feedback resistor RF has to carry some DC source current in addition to the I/ß collector current component. This current tends to force the emitter voltage of Q2 and thus the collector voltage of Q1 to be increased. The 'pull-up' resistor RX is added to help in this regard; it enables some of the DC current to be supplied by VCC directly, in lieu of having it flow through RF. (This can be appreciated from a node equation written at the Q1 base.)

Anticipate (and subsequently verify for your design) that the Q2 base current can be neglected compared to the current in RC1. Write a loop equation in terms of the Q1 collector current I as indicated in the figure. Neglecting the Q2 base current justifies substitution of the current in RC1 for the Q1 collector current. The result is a single equation with a single unknown whose terms can be rearranged as



The term in parentheses in the numerator is the difference between the part of the current in RX to go to the base and that to go to RS, i.e., away from the base. This difference

$$I = \frac{VCC - 2VBE + RF\left(\frac{VCC - VBE}{RX} - \frac{VBE}{RS}\right)}{RC1 + \frac{RF}{ß}}$$

would be provided through RF, and should be designed (approximately) to be zero. Note the prominent suggestion (in the denominator of the equation) that to reduce the influence of variations of ß the design should make ß RC1 >> RF.

An estimate of the voltage gain can be made as

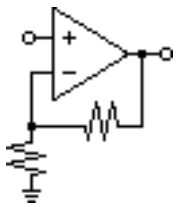
Voltage Gain ≈ (-RF/RS)(RC2/RE2)

The first factor corresponds to the shunt feedback for the first stage; as noted before the effect of the emitter connection of RF should be essentially the same electrically as if the connection were made to the collector of Q1. The second factor corresponds to series feedback for the second stage.

Design a Shunt-Series Pair amplifier to produce a nominal 2v peak output voltage at 1 kHz. Use Vcc = 10v, RS = 1KΩ. Use 2N3904 transistors (ß≈ 120, VBE ≈ 0.7v. Compare calculated bias voltages and currents with computed values. Verify explicitly all design assumptions made.

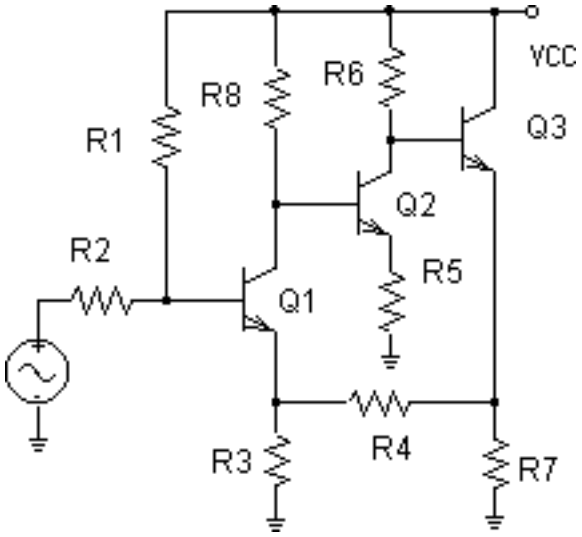
In general selecting a parameter value so as to improve one aspect of circuit performance almost always degrades performance in another aspect. In this respect comment critically in the report on the suggestion that making RE2 -> 0 increases the gain. Alternatively will making RC2 open-circuit increase gain?

(D) Series-Shunt FB Pair Amplifier



It generally helps in designing a circuit to have some overall organizing principle in mind to guide the design. The non-inverting idealized opamp configuration drawn to the right provided that guidance here for the design of a discrete BJT form of the amplifier using a Series-Shunt feedback pair.

A circuit so designed is drawn below. Q1 and Q2 form a non-inverting amplifier, and Q3 is an emitter follower added to provide the feedback current without loading the Q2 collector excessively. Following an inference from the idealized amplifier the emitter current of Q1 is designed to be small compared to the current in the emitter resistance R3; a concomitant implication is that most of the current in R3 is to be provided through the feedback resistance R4. This assumption simplifies the circuit analysis/design.



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Anticipating (and subsequently verifying) the Q1 base current to be small compared to the current in the bias resistors R1 and R2 the Q1 base voltage can be readily estimated, and from this the current in R3 can be calculated. If essentially all this current is to be provided through R4 the emitter voltage of Q3 (and the Q3 emitter current) can be determined. The Q2 collector voltage follows as well.

The collector current of Q2 (neglecting the Q3 base current) is estimated next; the Q3 emitter current is essentially the same, and so theQ2 base voltage follows. This enables the Q1 collector current to be determined. The Q1 emitter current is approximately the same as the collector current, and if this is arguably ‘small’ compared to the current in the emitter resistor the calculation is consistent.

Assume VCC is 15volts, R1 = 150KΩ, R2 = 10kΩ, and Q1,Q2 are 2N3904 (ß ≈ 120, VBE ≈ 0.7v). Design an amplifier to provide a nominal incremental voltage gain > 10 (20 dB).at 10 kHz.

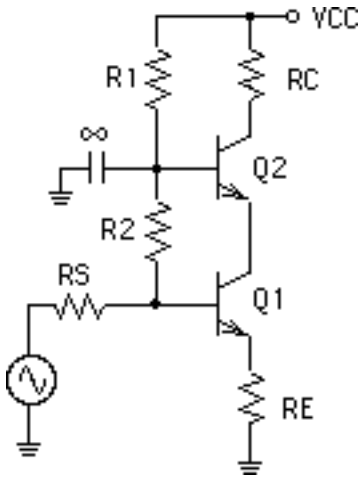
Use the simplified large-signal BJT model in describing your design selections. **Be sure** to present explicit justification for each assumption on which your calculations are based. Estimate the AC voltage gain. Use PSpice to compute the DC bias voltages and currents, and the AC voltage gain. Comment meaningfully on the relationship between calculated estimates and computed values. Comment on the voltage gain estimated by the 'opamp' viewpoint.

Changes in the Q2 collector voltage and the Q3 emitter voltage are essentially equal since the Q3 junction voltage does not vary greatly. Hence the argument might be made that the feedback resistor R4 can be connected directly to the Q2 collector, eliminating the need for Q3, without changing the voltage gain. Comment critically on this suggestion. What role does Q3 play in the circuit?

If the AC voltage gain is in fact determined largely by the ratio of the feedback resistance and the Q1 emitter resistance why not increase the one and decrease the other? Clearly open-circuiting the one and/or short-circuiting the other doesn't seem quite right. Comment critically on this suggestion.

(E) Cascode Amplifier

The two-stage 'cascode' amplifier configuration consists of a Common Emitter input stage and a Common Base second stage. The first stage (Q1) operates as a current amplifier, while the second stage provides a low input-resistance loading and (nearly) unity current gain transfer to the output resistance. This configuration provides a reduced internal capacitive coupling between input and output, improving high frequency performance. However details of this enhancement are not considered here.



An illustrative cascode amplifier circuit diagram is drawn to the right. The capacitor at the base of Q2 provides an AC ground for the (high) frequency range of interest, so that in so far as <u>incremental</u> behavior is concerned the performance is that of a CE stage followed by a CB stage. The circuit configuration provides a compact coordinated DC biasing of the two stages.

To simplify the design of this circuit the current in the resistive bias network may intentionally be made much larger than the transistor base currents. For this condition, i.e., neglecting the base currents, the bias network operates essentially as a resistive voltage divider. This enables a quick estimate of the Q1 base voltage, and from this an estimate of the Q1 emitter current. The collector voltage of Q1 may be estimated from the Q2 base voltage. The emitter/collector currents of Q1 and Q2 will be approximately equal.

The incremental voltage gain may be estimated as:

$$\frac{R2}{R2 + RS} \quad \frac{1}{RE} \quad RC$$

The first term is the voltage input transfer (resistance divider) loss from the source to the base of Q1. Essentially all the base voltage appears across RE (anticipating ß RE >> rbe), and the Q2 collector current is approximately the same as the Q1 emitter current. A more precise estimate (or justification for this estimate) can be made using the incremental parameter equivalent circuit

Assume Q1, Q2 are 2N3904; ß ≈ 120,VBE ≈ 0.7v. Use RS = 4.7kΩ, and VCC = 10v. Design an amplifier to amplify a 5kz sine wave

Estimate the DC bias voltages and currents for your design. Use the simplified large-signal BJT model and be sure to present <u>explicit</u> justification for <u>each</u> assumption based on your calculations. Estimate the AC voltage gain.

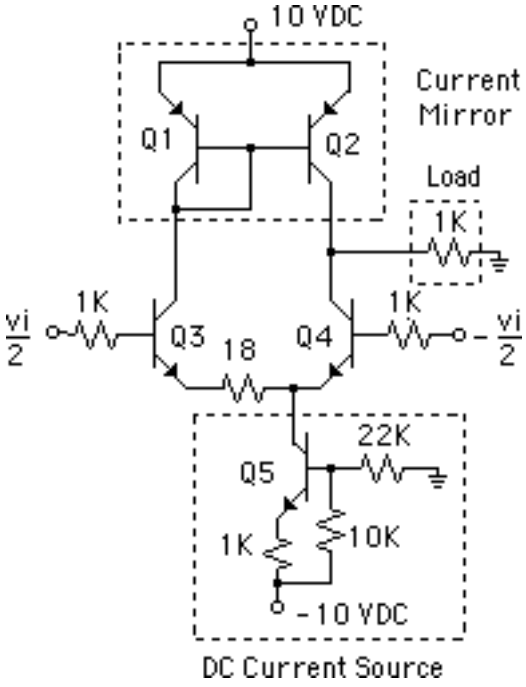
Use PSpice to compute the DC bias voltages and currents, and the AC voltage gain

The capacitor is specified indirectly, i.e. it is to be large enough to be an AC short-circuit at frequencies of interest. Assume a <u>minimum</u> signal frequency of 100Hz. Specify an appropriate capacitance, and support your choice (without referring to a PSpice computation to show 'it works').

The voltage gain is proportional to the Q2 load resistance. Respond critically to the suggestion that this resistance be increased by a factor of 10 to obtain an order of magnitude increase in gain

(F) Differential Amplifier ********** Review This

The advent of the integrated circuit led to the development of circuit configurations that used the strengths of monolithic technology to advantage. The high degree to which the characteristics of like components on the same substrate can be matched led to extensive use of symmetry as a filtering mechanism. The differential amplifier circuit configuration in particular assumed considerable prominence in this respect. An illustrative differential circuit is drawn to the right, with a 'differential mode' signal applied.



Transistors Q3 and Q4 form the basic differential input pair, with bias current provided by the 'current source' formed by Q5. Q1 and Q2 provide a current 'mirror' to transfer the collector current of Q3 to the Q4 collector path. Because of the difference in the Q1, Q2 collector voltages the Early Effect will cause the DC collector current of Q2 to be somewhat higher than that of Q1, and this causes a net quiescent current through the 1kΩ load resistor. To correct for this, so that the DC bias current through the 1kΩ load is essentially zero, a 'balancing' resistor is added to the Q3 emitter. (Ordinarily a potentiometer would connect the Q3-Q4 emitters, with the Q5 collector connected to the center-tap; the adjustment would be experimental.) Because of the voltage drop across the 18Ω the emitter junction voltage of Q3 is a bit lower than that of Q4, making the Q3 collector current somewhat lower than that of Q4. The increase in the Q2 current over that of Q1 because of the Early Effect is thus offset by this decrease in Q3 bias current.

An incremental increase in Q3 collector current (more current into the collector) is mirrored by Q2, and flows towards the load. The corresponding incremental decrease in Q4 collector current also flows towards the load. The net load current is the sum of these currents.

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Assume Q1, Q2, Q3,and Q4 are 2N3904; ß ≈ 120,VBE ≈ 0.7v. Use VCC = 10v. Design an amplifier to amplify a 5kz sine wave

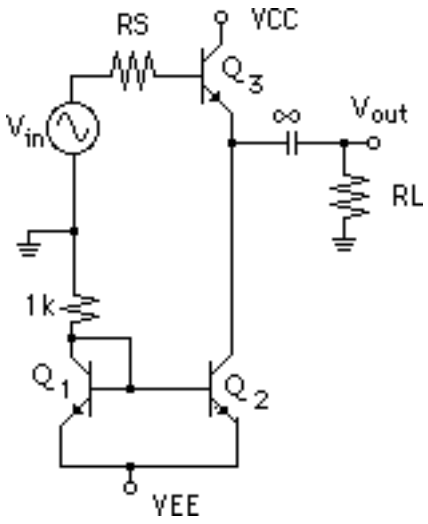
Estimate the DC bias voltages and currents for your design. Use the simplified large-signal BJT model and be sure to present explicit justification for each assumption based on your calculations. Estimate the AC voltage gain.

Use PSpice to compute the DC bias voltages and currents, and the AC voltage gain

The capacitor is specified indirectly, i.e. it is to be large enough to be an AC short-circuit at frequencies of interest. Assume a minimum signal frequency of 100Hz. Specify an appropriate capacitance, and support your choice (without referring to a PSpice computation to show 'it works').

The voltage gain is proportional to the Q2 load resistance. Respond critically to the suggestion that this resistance be increased by a factor of 10 to obtain an order of magnitude increase in gain

(G) **Emitter Follower**



The circuit diagram to the right is a vartiant of an emitter follower amplifier. Q1 is configured as a diode-connected transistor, and in conjunction with Q2 forms a current mirror used to approximate a DC current source in the emitter of Q3. Q3 is used as an emitter follower to drive the 50Ω load RLfrom the signal source. If a load resistance RL<<RS were connected directly to the signal source there would be a considerable reduction in the signal amplitude in the transfer from source to load. The emitter follower presents a high input resistance and a low output resistance to provide an efficient voltage transfer..

Given VCC = 12v, VEE = -12v, RS = 1kΩ and RL = 50Ω. Design an emitter follower to obtain nominal unity voltage gain. Use 2N3904 transistors, ß ≈ 120, VBE ≈ 0.7v.

Estimate the DC branch currents and voltages using the simplified large-signal BJT model. Include an estimate for the Q3 emitter voltage. Provide explicit justification for each assumption made, using the results of your calculations.

Draw the incremental parameter equivalent circuit (use the simplified model) and calculate the AC voltage gain. Compare this gain with the gain were the load connected directly to the source.

Use PSpice to compute the DC bias voltages and currents, and the AC voltage gain. Compare (and evaluate) the calculated and computed values.

Suppose V_{in} is a 1 kHz sinusoid with amplitude 0.75v. Compute (and plot) V_{out} on the same axes as V_{in} for about 2 milliseconds. Explain the differences. What sort of adjustments would you suggest (include reasons for suggestions)?