# ECE/CS 5780/6780: Embedded System Design

Chris J. Myers

Lecture 20: Memory Interfacing

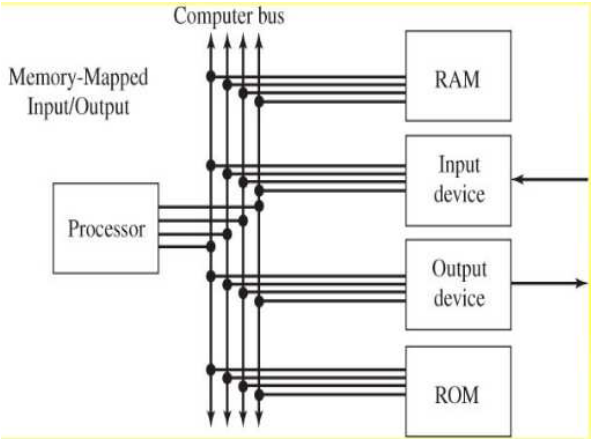


## Introduction

- Most embedded systems use only the memory built-in to the microcontroller.
- Memory interfacing and bus timing is important to understanding internal microcontroller architecture.
- Sometimes internal memory insufficient, and external memory needed.
- Sometimes external devices are interfaced using memory-mapped I/O.

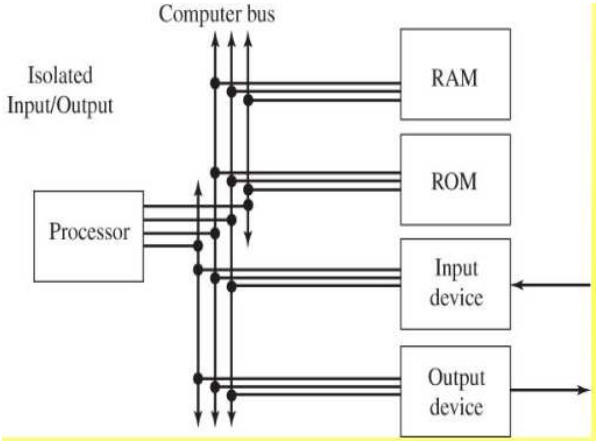


## Memory-Mapped I/O



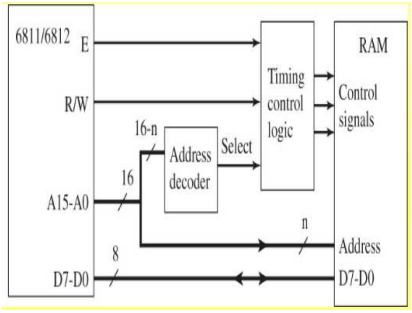



## Isolated I/O





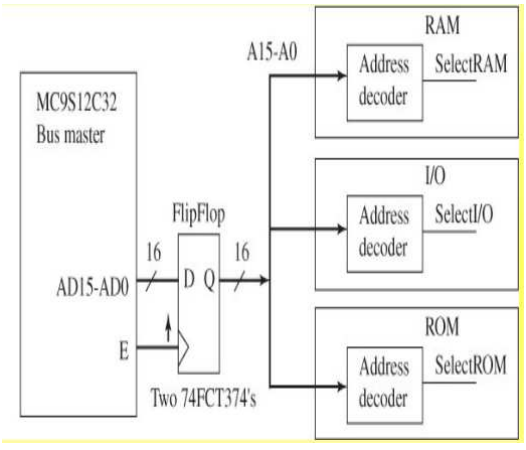

## Expanded Mode




| Select | R/W | Function |
|---|---|---|
| 0 | 0 | Off |
| 0 | 1 | Off |
| 1 | 0 | Write |
| 1 | 1 | Read |



## Multiplexed Address and Data Lines



## Full-Address Decoding

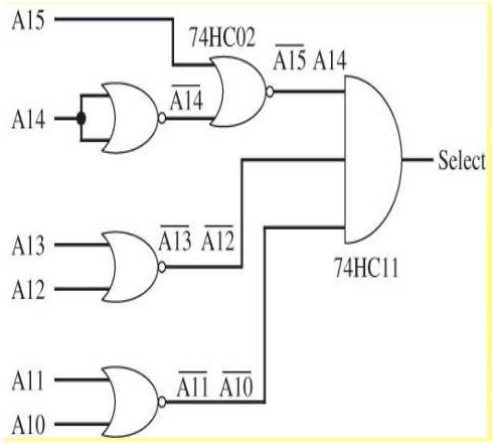
- *Slave* selected only when slave's address is on the bus.
- Design using the following steps:
  1. Write specified address using 0,1,X:
     `0100,00XX,XXXX,XXXX` for 1K RAM at $4000-$43FF
  2. Write equation using all 0s and 1s:

$$select = \overline{A15} \cdot A14 \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11} \cdot \overline{A10}$$

  3. Build circuit using gates.

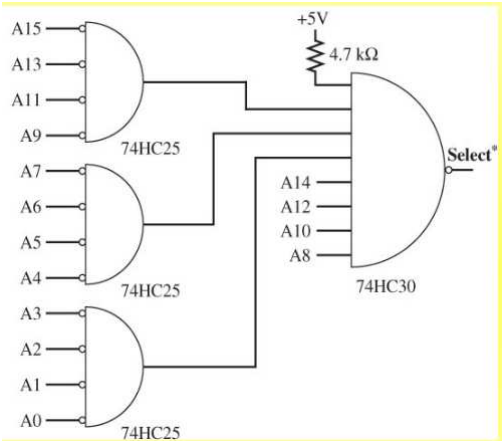


## Address Decoder for 1K RAM at $4000-$43FF






## An Address Decoder for I/O Device at $5500

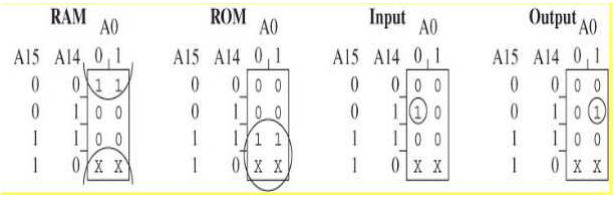





## Minimal-Cost Address Decoding

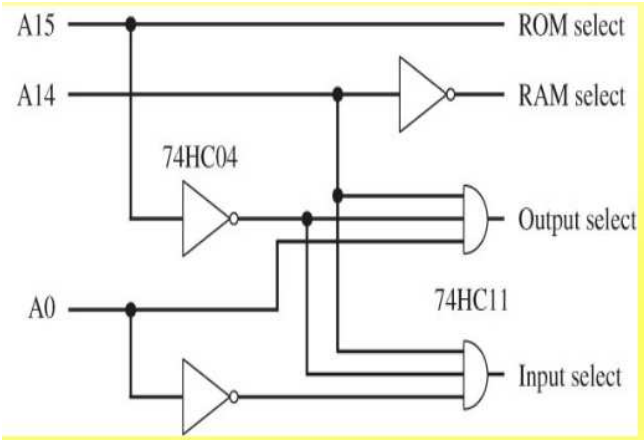
- Use don't cares for unspecified addresses to simplify.
- Example:

| | | |
|---|---|---|
| 4K RAM | $0000 to $0FFF | `0000,XXXX,XXXX,XXXX` |
| Input | $5000 | `0101,0000,0000,0000` |
| Output | $5001 | `0101,0000,0000,0001` |
| 16K ROM | $C000 to $FFFF | `11XX,XXXX,XXXX,XXXX` |



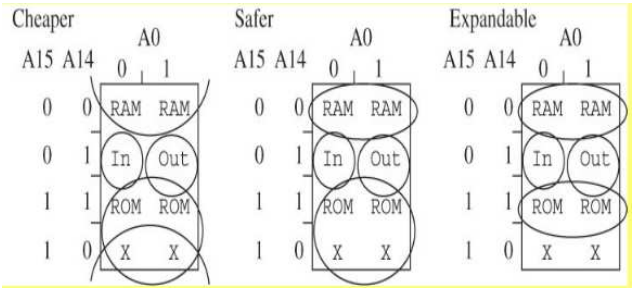



## An Address Decoder






## Karnaugh Maps



## Special Cases

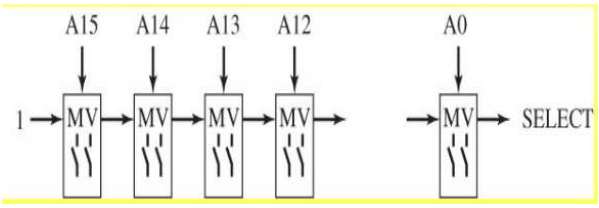
- Size of the memory is not a power of 2.
  20K RAM with address range \$0000 to \$4FFF

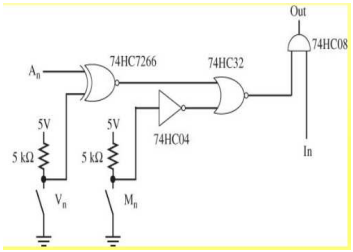
  `00XX,XXXX,XXXX,XXXX` Range \$0000 to \$3FFF
  `0100,XXXX,XXXX,XXXX` Range \$4000 to \$4FFF
- Start address divided by memory size not an integer.
  32K RAM with address range \$2000 to \$9FFF

  `001X,XXXX,XXXX,XXXX` Range \$2000 to \$3FFF
  `01XX,XXXX,XXXX,XXXX` Range \$4000 to \$7FFF
  `100X,XXXX,XXXX,XXXX` Range \$8000 to \$9FFF



## Programmable Address Decoder

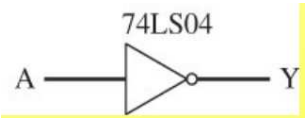



| In | Mn | An | Vn | Out |
|---|---|---|---|---|
| 0 | X | X | X | 0 |
| 1 | 0 | X | X | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |



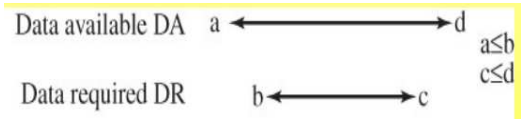
## Timing Intervals

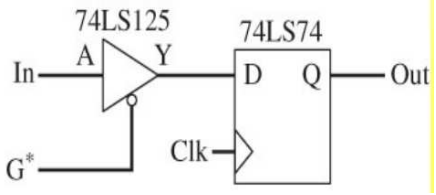



$$(\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + 10$$
$$(\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + [5, 15]$$
$$(\uparrow Y, \downarrow Y) = (\downarrow A + [8, 15], \uparrow A + [5, 12])$$



## Available and Required Time Intervals




$$DA = (\downarrow G^* + [10, 20], \uparrow G^* + [0, 15])$$
$$DA = (\downarrow G^* + 20, \uparrow G^*) \text{ worst-case}$$
$$DR = (\uparrow Clk - 30, \uparrow Clk + 5)$$

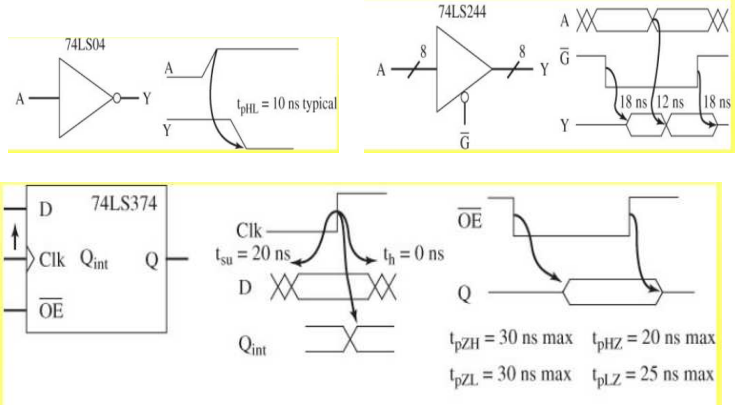


## Timing Diagrams

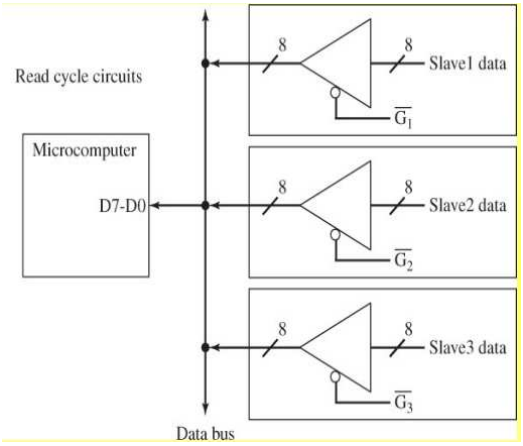
| Symbol | Input | Output |
|---|---|---|
| | The input must be valid | The output will be valid |
| | If the input were to fall | Then the output will fall |
| | If the input were to rise | Then the output will rise |
| | Don't care, it will work regardless | Don't know, the output value is indeterminate |
| | Nonsense | High impedence, tristate, HiZ, Not driven, floating |



## Example Timing Diagrams

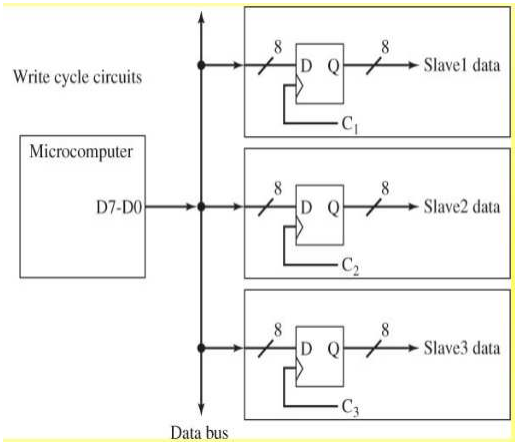


## Read Cycle Circuit



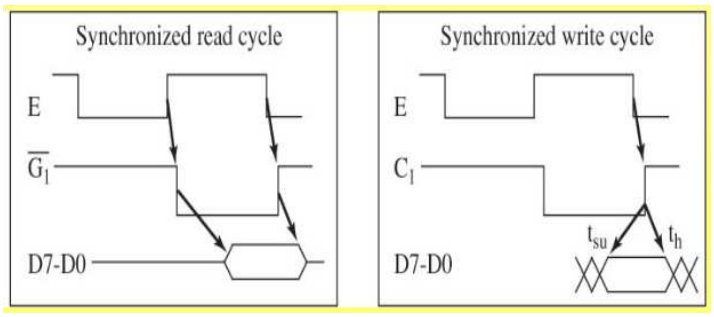



## Write Cycle Circuit



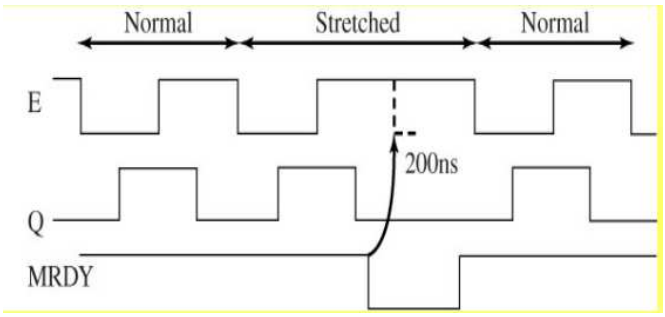



## Synchronous Bus Timing



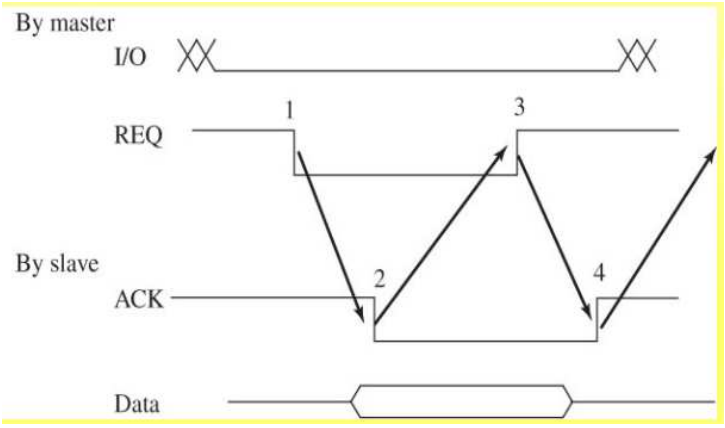



## Partially Asynchronous Bus Timing (6809/680x0/x86)



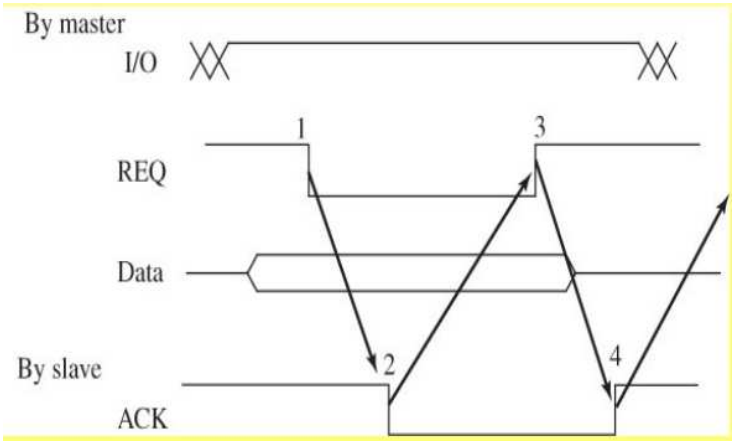



## Fully Asynchronous Read Cycle

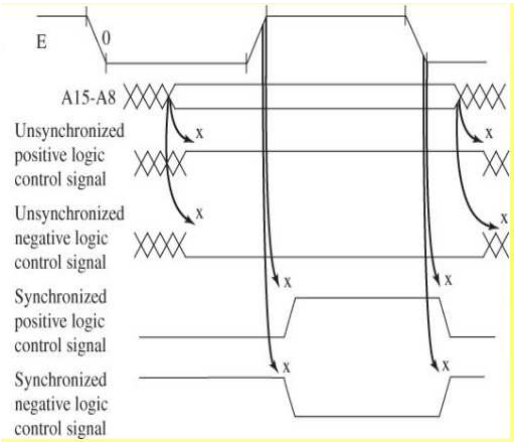





## Fully Asynchronous Write Cycle

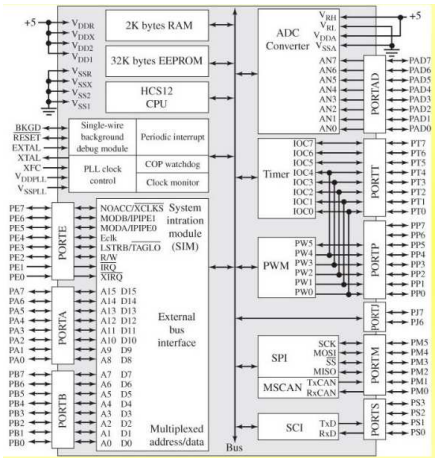


## Four Types of Control Signals






## MC9S12C32






## MC9S12C32 Modes of Operation

| BKGD | MODB | MODA | Description | Port A | Port B | MODx write |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Special Single chip | In/Out | In/Out | Write anytime, not peripheral |
| 0 | 0 | 1 | Emulation Exp. narrow | A15-A8/ D7-D0 | A7-A0 | Cannot change |
| 0 | 1 | 0 | Special test Exp. narrow | A15-A8/ D15-D8 | A7-A0 D7-D0 | Write anytime, not peripheral |
| 0 | 1 | 1 | Emulation Exp. wide | A15-A8/ D15-D8 | A7-A0 D7-D0 | Cannot change |
| 1 | 0 | 0 | Normal Single chip | In/Out | In/Out | Write once, Norm exp N/W |
| 1 | 0 | 1 | Normal Exp. narrow | A15-A8/ D7-D0 | A7-A0 | Cannot change |
| 1 | 1 | 0 | Peripheral | – | – | Cannot change |
| 1 | 1 | 1 | Normal Exp. wide | A15-A8/ D15-D8 | A7-A0 D7-D0 | Cannot change |

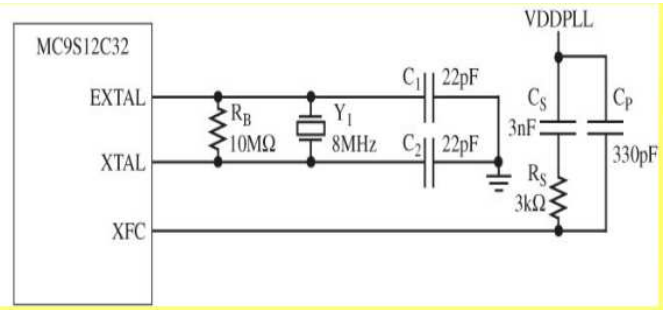


## MC9S12C32 Modes of Operation

| BKGD | MODB | MODA | Description | Port A | Port B | MODx write |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | Normal Single chip | In/Out | In/Out | Write once, Norm exp N/W |
| 1 | 0 | 1 | Normal Exp. narrow | A15-A8/ D7-D0 | A7-A0 | Cannot change |
| 1 | 1 | 1 | Normal Exp. wide | A15-A8/ D15-D8 | A7-A0 D7-D0 | Cannot change |

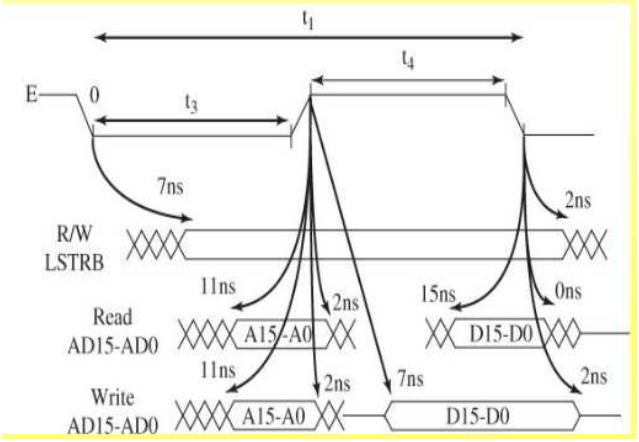


## MC9S12C32 Clock Circuit

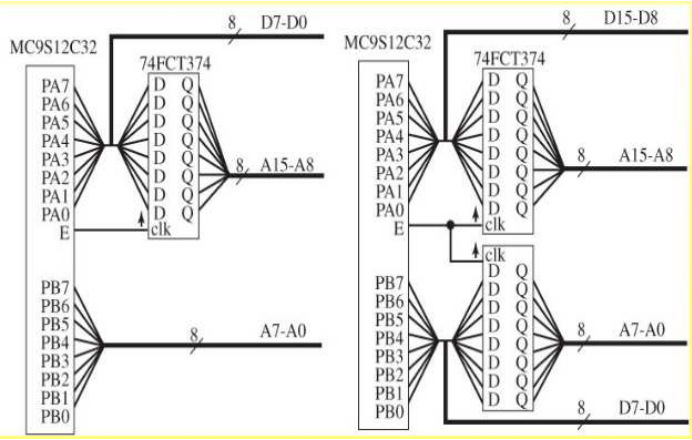





## MC9S12C32 Expanded Mode Bus Timing

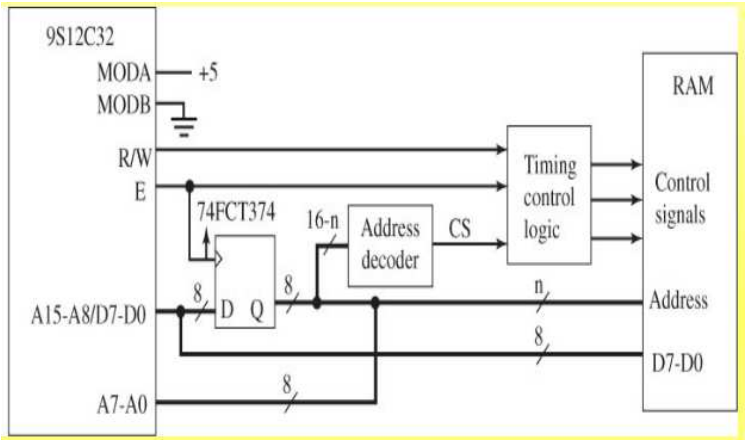


## Address Latch for MC9S12C32



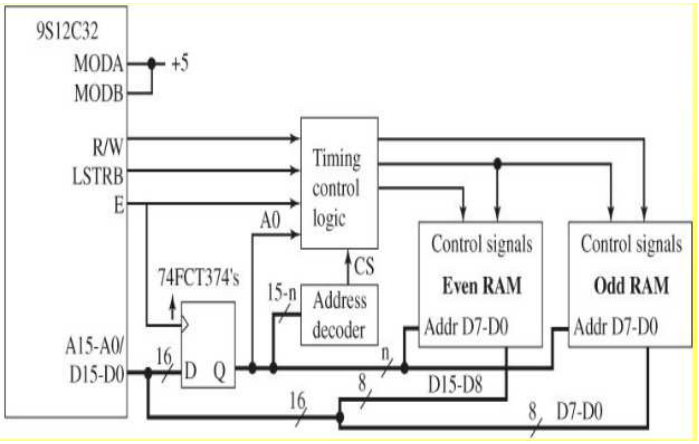



## General Approach to Memory Interfacing



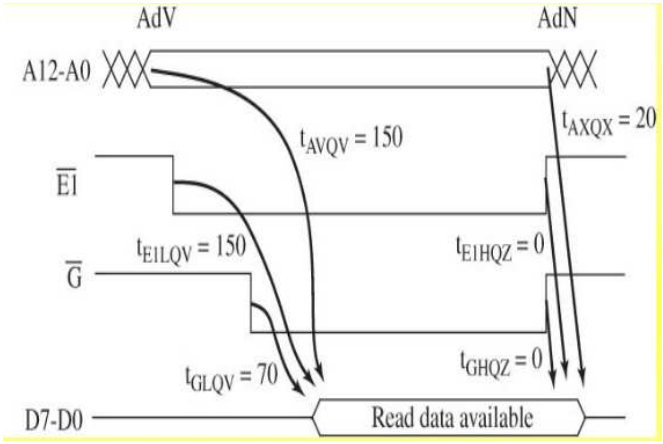



## Wide Expanded Mode



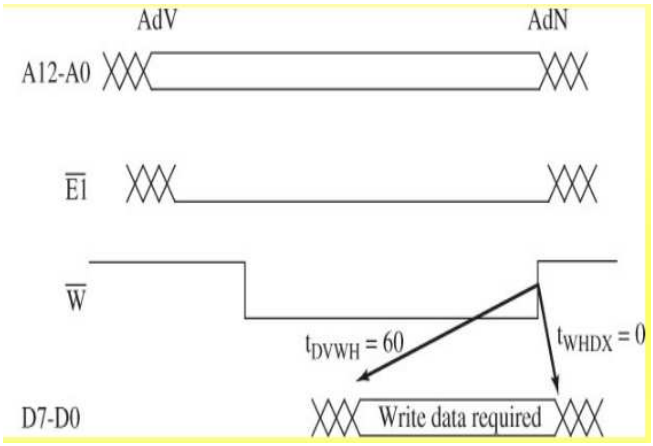



## 8K RAM Read Timing



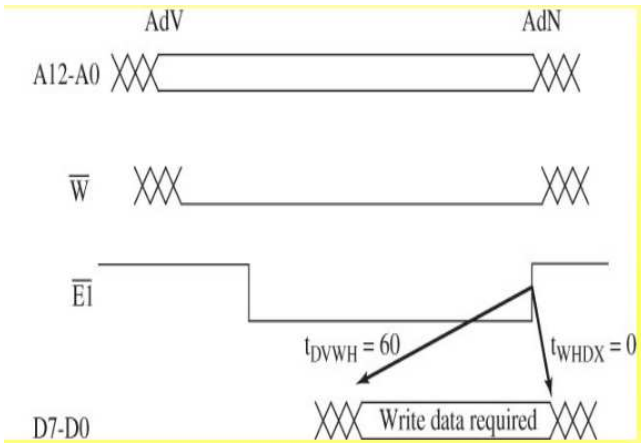



## 8K RAM Write Timing

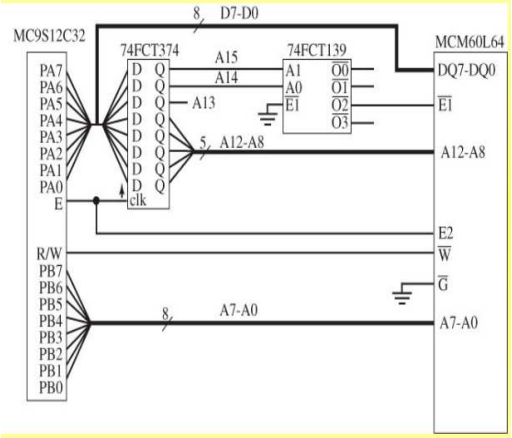





## 8K RAM Write Timing

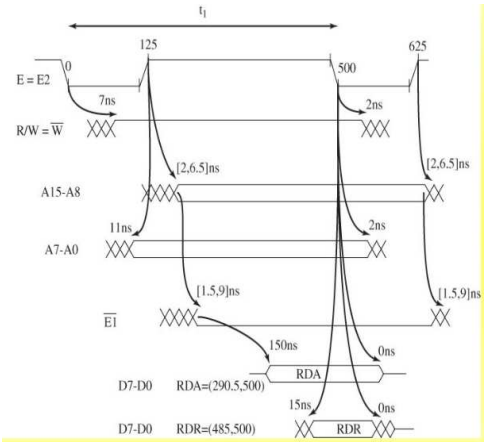


## 8K RAM Interface ($8000-$9FFF)



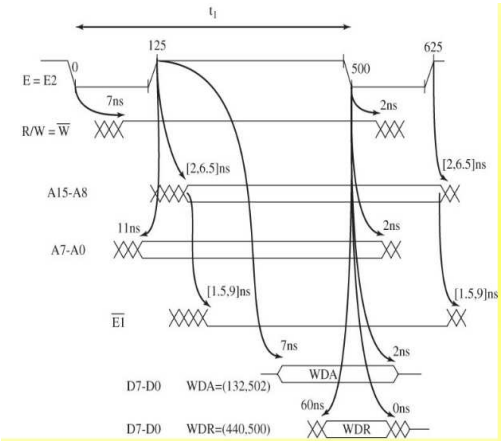



## 8K RAM Interface Read Timing



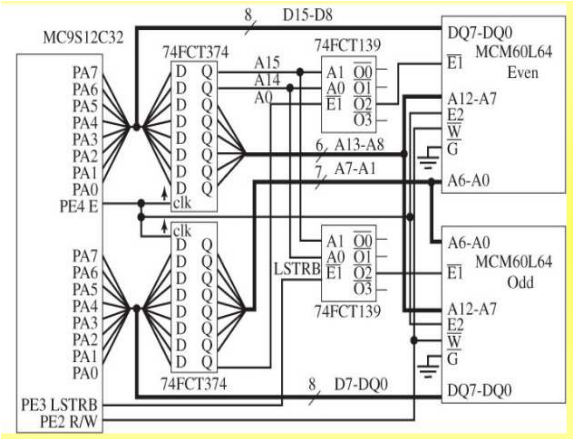



## 8K RAM Interface Write Timing






## 8K by 16-bit RAM Interface






## Dynamic RAM (DRAM)

| DRAMs | SRAMs |
|---|---|
| High density | Low density |
| One xtor, one cap./bit | 3-4 xtors/bit |
| Slower | Faster |
| High fixed cost (refresh) | Low fixed cost (address decoder) |
| Low incremental cost | Higher incremental cost |
| Address multiplexing | Direct addressing |