ATD Checkout Via UBUG12

(Put test Voltage on Pin AN7)

```
mm  82  80    ATDCTL2 ← #80   (Turn ON ATD subsection)
mm  83  08    ATDCTL3 ← #08   (Select Single Conversion Seq)
mm  84  07    ATDCTL4 ← #07   (Select 10-bit conv, 2 clk Sample
                               Time, 1/16 ATD Clock Prescale
[mm 85  87    ATDCTL5 ← #87   (Convert Ch 7)
 md 86        Read from ATDSTAT0
              check to ensure MSB = 1  (SCF Flag = 1)
                                       ⇒Conv. done!
 md 90 ⊙      Read result from #90:#91
              (ATDDR0H : ATDDR0L)]
```

(Next Conv.) → back to the `[mm 85 87` line

SPI Checkout Via UBUG12

(Assumed that the two 595's have been connected to MOSI (PM4), SCK (PM5), and RCLK (PM3))

SCK MOSI RCLK

```
mm  252 38    DDRM ← #38   (Make PM5, PM4, PM3 outputs)
mm  250 00    PTM ← #00    (Lower RCLK Pin)
mm  D8  5C    SPICR1 ← #5C {(Enable SPI, Make Master, Make
                            SCK rise in middle of data
                            bit time slots, disable SSI
                            so PM3 is general-purpose output
                            (RCLK Pin)
mm  DA  20    SPIBR ← #23   (1 MHz bit rate)
[md DB        ("single" "dummy" read of SPISR (Status Register)
                            To clear SPIF bit before sending data)
mm  DD  xx    SPIDR ← xx   (Send First data byte)
md  DB        (Loop on SPISR MSB (SPIF Bit) Until Set
                            indicating transmission is completed)
mm  DD  yy    SPIDR ← yy   (Send Second data byte)
md  DB        (Loop on SPISR MSB (SPIF Bit) Until Set)
mm  250 08    PTM ← #08    (Raise RCLK — Only NOW
mm  250 00    PTM ← #00}    can shifted result be
                            read at 74HC595 output
                            pins!)
                           (Lower RCLK.)
```

→ back to the `[md DB` line