

MC9S12C-Family

Product Proposal

16-Bit Microcontroller

Based on Motorola's market-leading flash technology, members of the MC9S12C-Family deliver the power and flexibility of our 16 Bit core (CPU12) family to a whole new range of cost and space sensitive, general purpose Industrial and Automotive network applications. MC9S12C-Family members are comprised of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 128K bytes of Flash EEPROM or ROM, up to 4K bytes of RAM, an asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an 8-channel 16-bit timer module (TIM), a 6-channel 8-bit Pulse Width Modulator (PWM), an 8-channel, 10-bit analog-to-digital converter (ADC) and up to one CAN 2.0 A, B software compatible module (MSCAN12). The MC9S12C-Family has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 10 dedicated I/O port bits are available with Wake-Up capability from STOP or WAIT mode. The MC9S12C-Family is available in 48, 52 and 80 pin QFP packages, with the 80 Pin version pin compatible to the HCS12 B and D- Family derivatives.

The C-Family includes ROM versions MC3S12C128/96/64/32/16 of all devices which provide a further cost reduction path for applications with high volume and stable code.

Features

- **16-bit HCS12 CORE**
 - HCS12 CPU
 - MMC (memory map and interface)
 - INT (interrupt control)
 - BDM (background debug mode)
 - DBG12 (enhanced debug12 module including breakpoints and change-of-flow trace buffer)
 - Multiplexed Expansion Bus (available only in 80 pin package version)
- **16-bit HCS12 CPU**
 - Upward compatible with M68HC11 instruction set
 - Interrupt stacking and programmer's model identical to M68HC11
 - Instruction queue
 - Enhanced indexed addressing
- **Wake-up interrupt inputs**
 - Up to 10-port bits available for wake up interrupt function
- **Memory options**
 - 16K, 32K, 64K, 96K and 128K Byte Flash EEPROM (erasable in 512-byte sectors) or
 - 16K, 32K, 64K, 96K and 128K Byte ROM
 - 2K and 4K Byte RAM
- **Analog-to-Digital Converters**
 - One 8-channel module with 10-bit resolution.
 - External conversion trigger capability
- **Up to one 1M bit per second, CAN 2.0 A, B software compatible modules**
 - Five receive and three transmit buffers

This document contains information on a new product. Specifications and information herein are subject to change without notice.



- Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
- Four separate interrupt channels for receive, transmit, error and wake-up
- Low-pass filter wake-up function
- Loop-back for self test operation

• **Timer Module (TIM)**

- 16-bit Counter with 7-bit Prescaler
- 8 programmable input capture or output compare channels
- Simple PWM Mode
- Modulo Reset of Timer Counter
- 16-Bit Pulse Accumulator
- External Event Counting
- Gated Time Accumulation

• **6 PWM channels**

- Programmable period and duty cycle
- 8-bit 6-channel or 16-bit 3-channel
- Separate control for each pulse width and duty cycle
- Center-aligned or left-aligned outputs
- Programmable clock select logic with a wide range of frequencies
- Fast emergency shutdown input

• **Serial interfaces**

- One asynchronous serial communications interface (SCI)
- One synchronous serial peripheral interface (SPI)

• **CRG (Clock Reset Generator Module)**

- Windowed COP watchdog,
- Real time interrupt,
- Clock monitor,
- Clock generation
- Reset Generation
- Phase-locked loop clock frequency multiplier
- Limp home mode in absence of external clock
- Low power 0.5 to 16 MHz crystal oscillator reference clock

• **Operation frequency**

- 32MHz equivalent to 16MHz Bus Speed for single chip
- 32MHz equivalent to 16MHz Bus Speed in expanded bus modes
- Option: 50MHz equivalent to 25MHz Bus Speed

• **Internal 2.5V Regulator**

- Supports an input voltage range from 3.3V-10% to 5.5V
- Low power mode capability
- Includes low voltage reset (LVR) circuitry
- Includes low voltage interrupt (LVI) circuitry

• **48-Pin LQFP, 52-Pin LQFP or 80-Pin QFP package**

- Up to 58 I/O lines with 5V input and drive capability
- Up to 2 dedicated 5V input only lines (IRQ, XIRQ)
- 5V A/D converter inputs and 5V I/O

• **Development support**

- Single-wire background debug™ mode (BDM)
- On-chip hardware breakpoints
- Enhanced DBG12 debug features

Table 1 List of MC9S12C-Family members

| Flash | ROM | RAM | Package | Device | CAN | SCI | SPI | A/D | PWM | Timer | I/O |
|-------|------|-----|---------|------------|-----|-----|-----|-----|-----|-------|-----|
| 128K | 0 | 4K | 48LQFP | MC9S12C128 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC9S12C128 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC9S12C128 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 96K | 0 | 4K | 48LQFP | MC9S12C96 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC9S12C96 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC9S12C96 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 64K | 0 | 4K | 48LQFP | MC9S12C64 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC9S12C64 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC9S12C64 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 32K | 0 | 2K | 48LQFP | MC9S12C32 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC9S12C32 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC9S12C32 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 32K | 0 | 2K | 48LQFP | MC9S12GC32 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC9S12GC32 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| 16K | 0 | 2K | 48LQFP | MC9S12GC16 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC9S12GC16 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| 0 | 128K | 4K | 48LQFP | MC3S12C128 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC3S12C128 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC3S12C128 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 0 | 96K | 4K | 48LQFP | MC3S12C96 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC3S12C96 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC3S12C96 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 0 | 64K | 4K | 48LQFP | MC3S12C64 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC3S12C64 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC3S12C64 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 0 | 32K | 2K | 48LQFP | MC3S12C32 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC3S12C32 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| | | | 80QFP | MC3S12C32 | 1 | 1 | 1 | 8ch | 6ch | 8ch | 60 |
| 0 | 32K | 2K | 48LQFP | MC3S12GC32 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC3S12GC32 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 35 |
| 0 | 16K | 2K | 48LQFP | MC9S12GC16 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 31 |
| | | | 52LQFP | MC9S12GC16 | 0 | 1 | 1 | 8ch | 6ch | 8ch | 35 |

• Pin out explanations:

— I/O is the sum of ports capable to act as digital input or output.

For 80 Pin Versions:

Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 8, S = 4, T = 8, PAD = 8.

12 inputs provide Interrupt capability (P= 8, J = 2, IRQ, XIRQ)

For 52 Pin Versions:

Port A = 3, B = 1, E = 2 + 2 input only, M = 6, P = 3, S = 2, T = 8, PAD = 8.

5 inputs provide Interrupt capability (P= 3, IRQ, XIRQ)

For 48 Pin Versions:

Port A = 1, B = 1, E = 2 + 2 input only, M = 6, P = 1, S = 2, T = 8, PAD = 8.

3 inputs provide Interrupt capability (P= 1, IRQ, XIRQ)

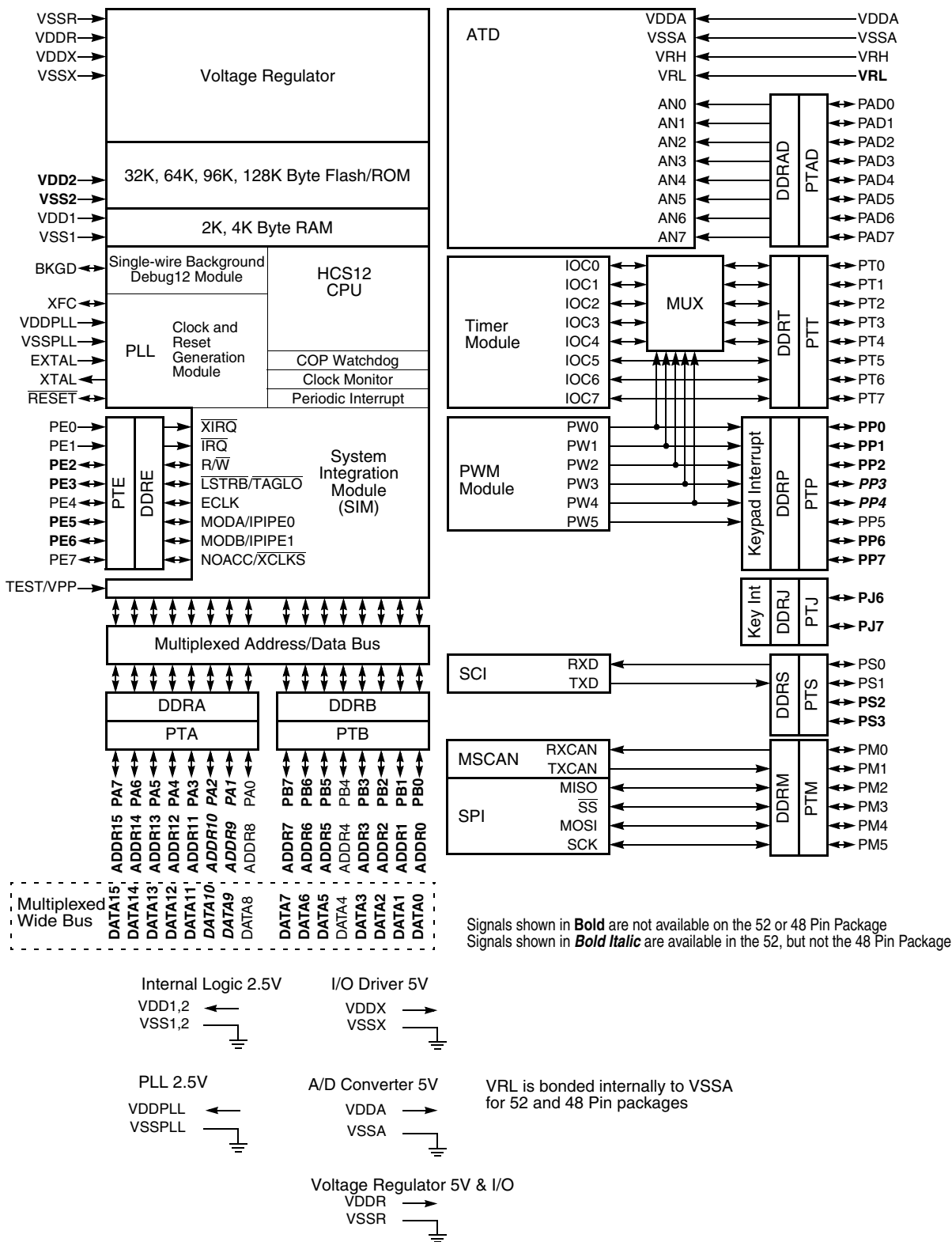
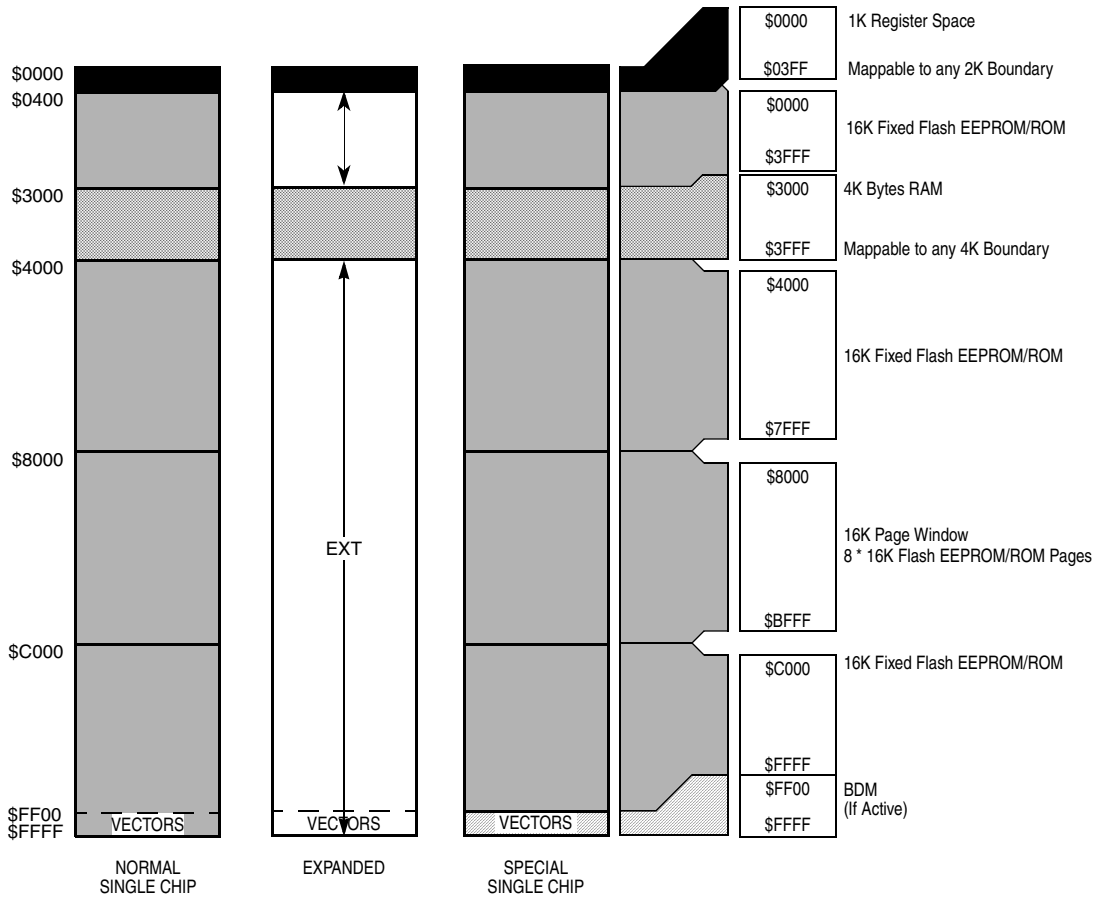


Figure 1 Block Diagram

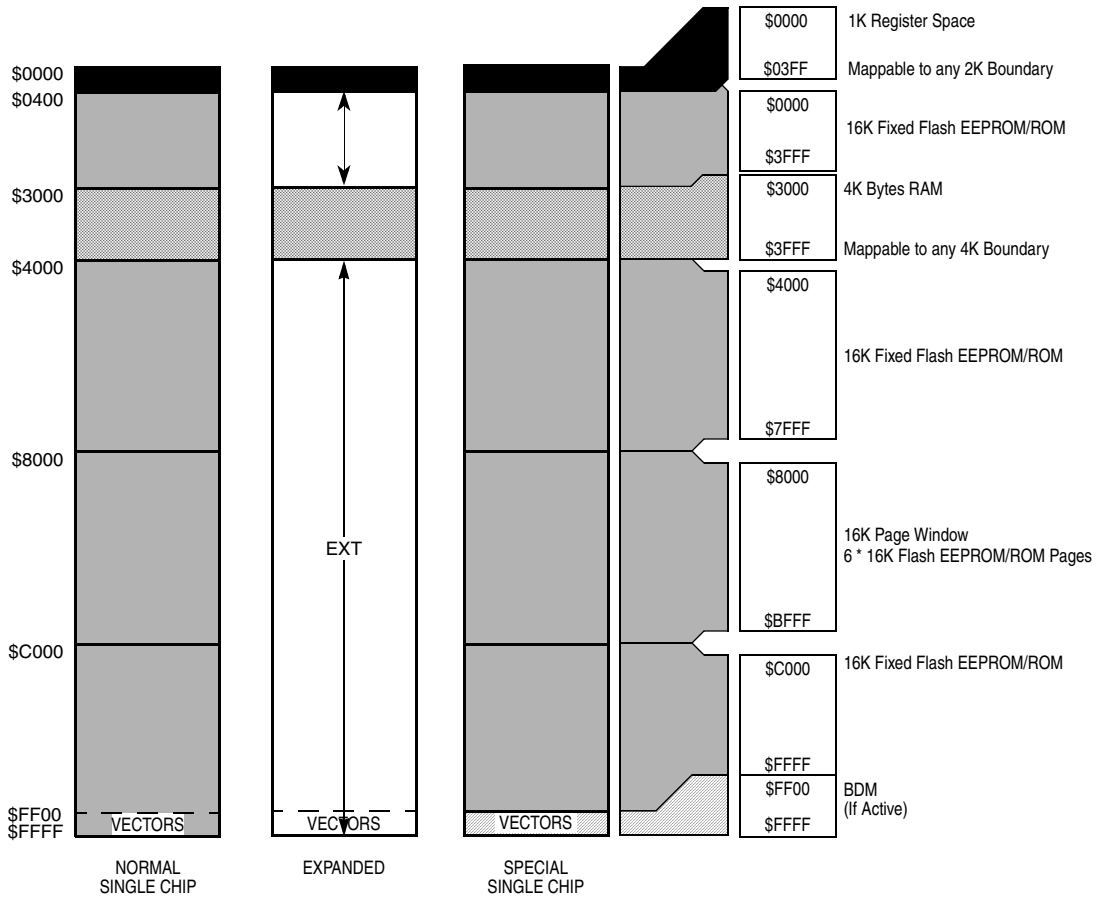


The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0000 - \$0FFF: 4K RAM (only 3K visible \$0400 - \$0FFF)

Flash Erase Sector Size is 1024 Bytes

Figure 2 MCxS12C128 User Configurable Memory Map

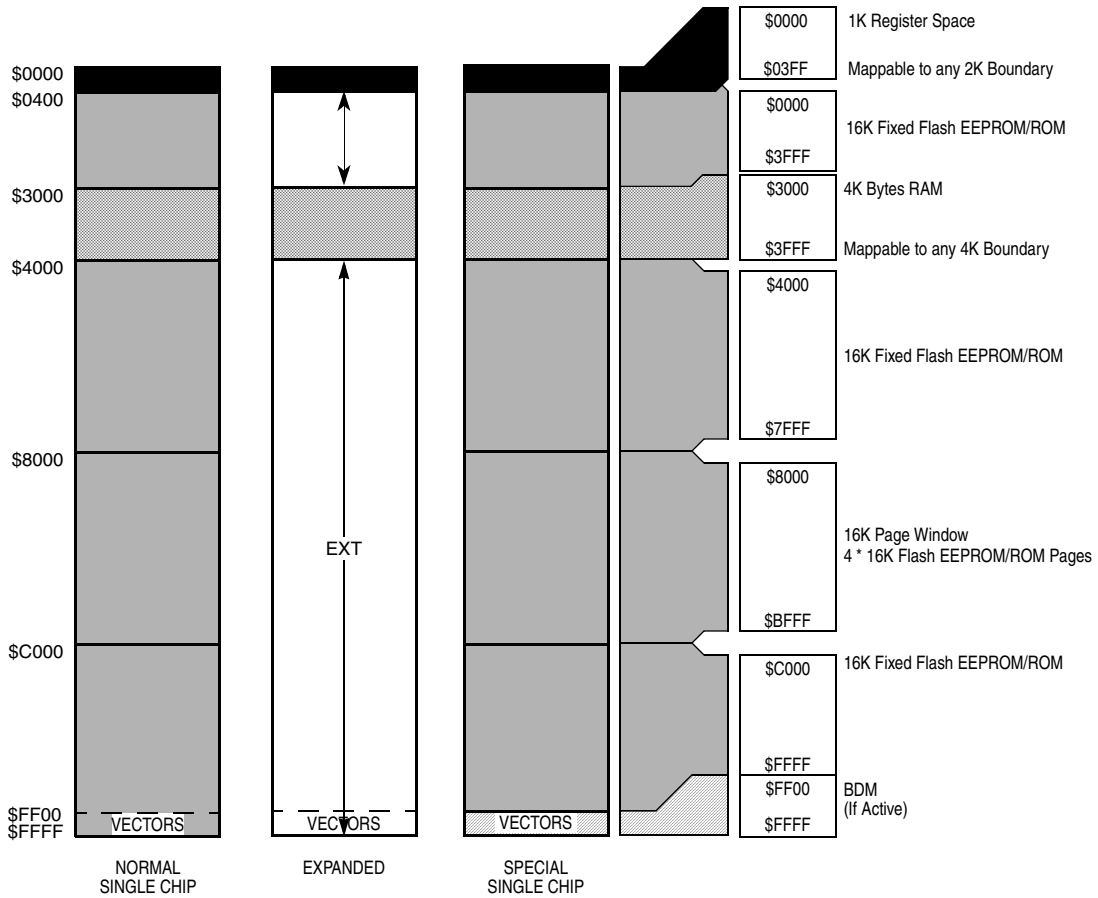


The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0000 - \$0FFF: 4K RAM (only 3K visible \$0400 - \$0FFF)

Flash Erase Sector Size is 1024 Bytes

Figure 3 MCxS12C96 User Configurable Memory Map

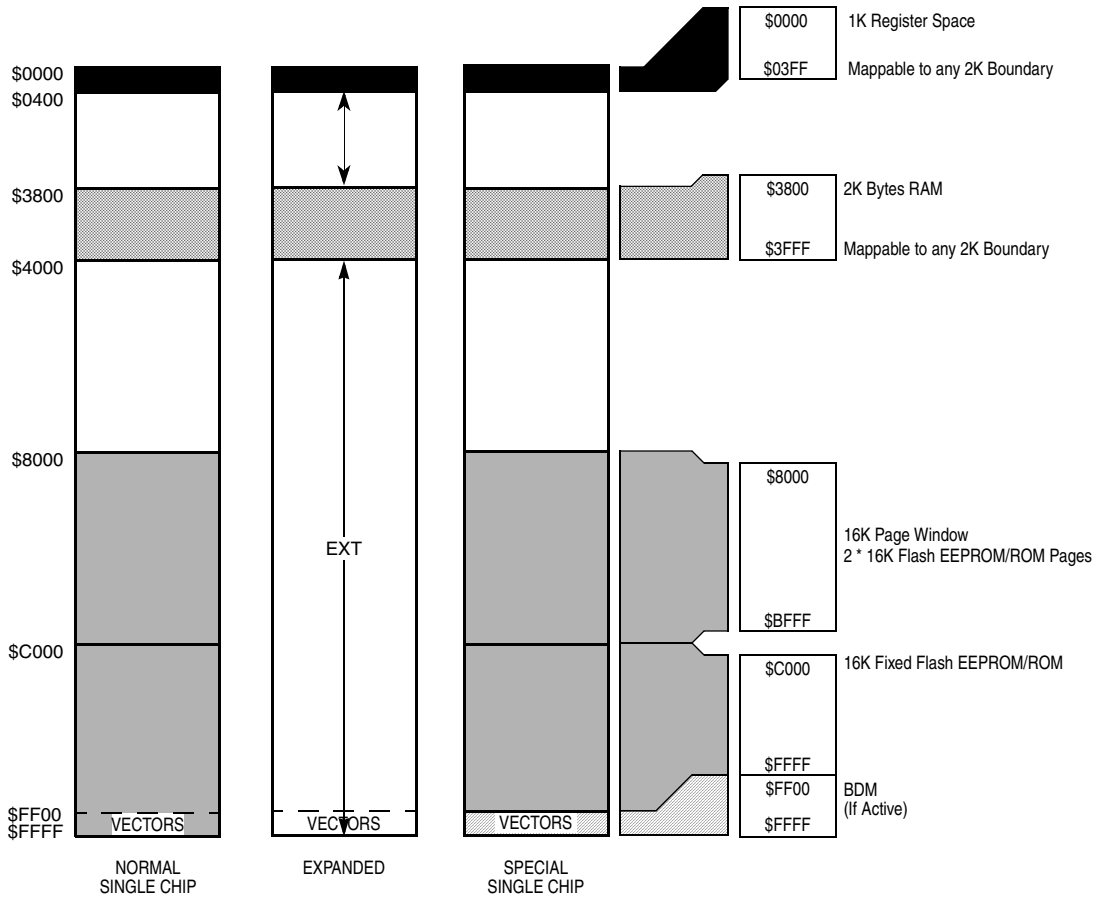


The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0000 - \$0FFF: 4K RAM (only 3K visible \$0400 - \$0FFF)

Flash Erase Sector Size is 512 Bytes

Figure 4 MCxS12C64 User Configurable Memory Map

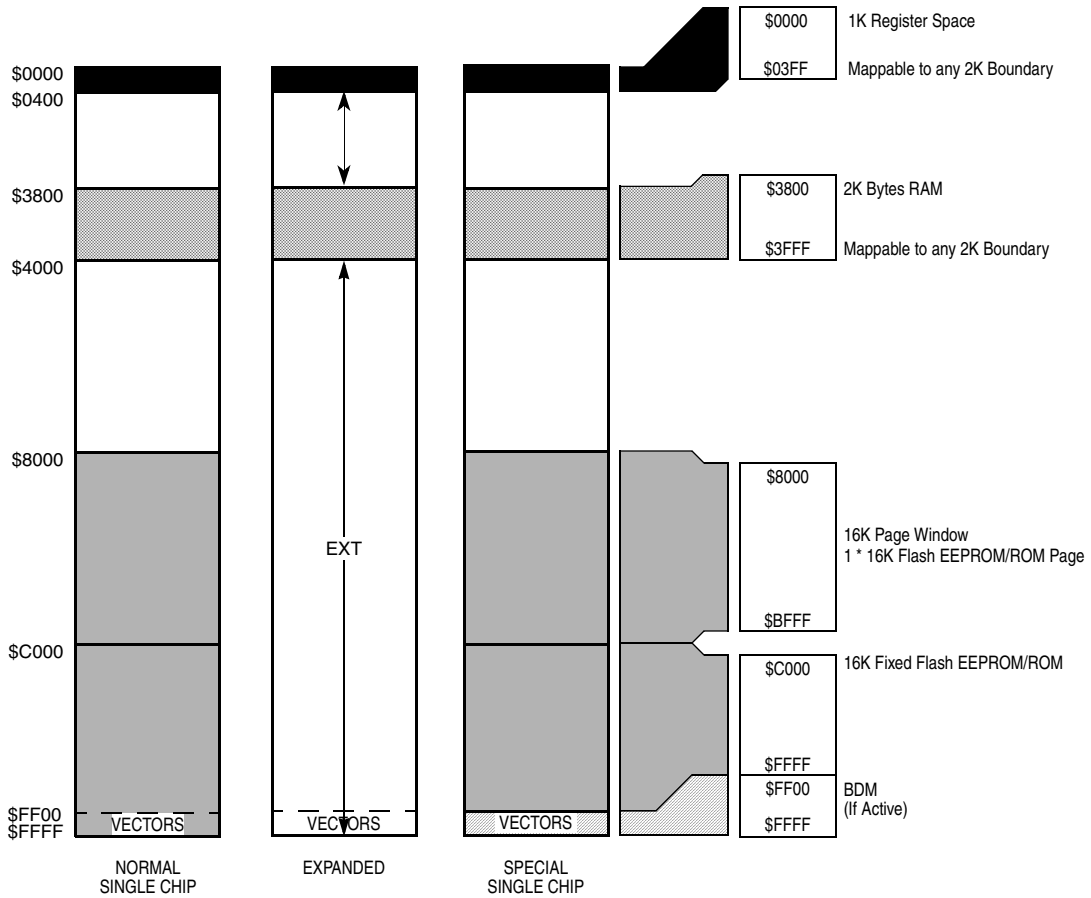


The figure shows a useful map, which is not the map out of reset. After reset the map is:

\$0000 - \$03FF: Register Space
 \$0800 - \$0FFF: 2K RAM

Flash Erase Sector Size is 512 Bytes

Figure 5 MCxS12C32 User Configurable Memory Map

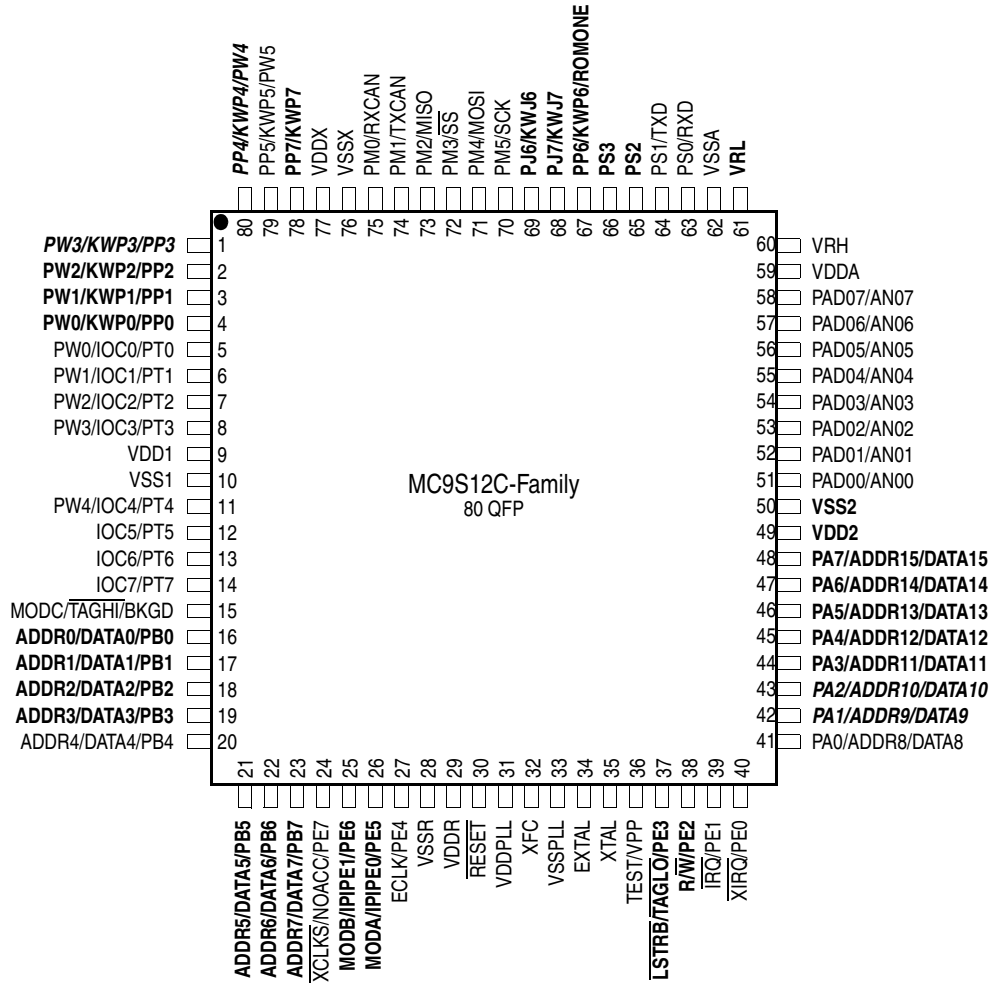


The figure shows a useful map, which is not the map out of reset. After reset the map is:

\$0000 - \$03FF: Register Space
 \$0800 - \$0FFF: 2K RAM

Flash Erase Sector Size is 512 Bytes

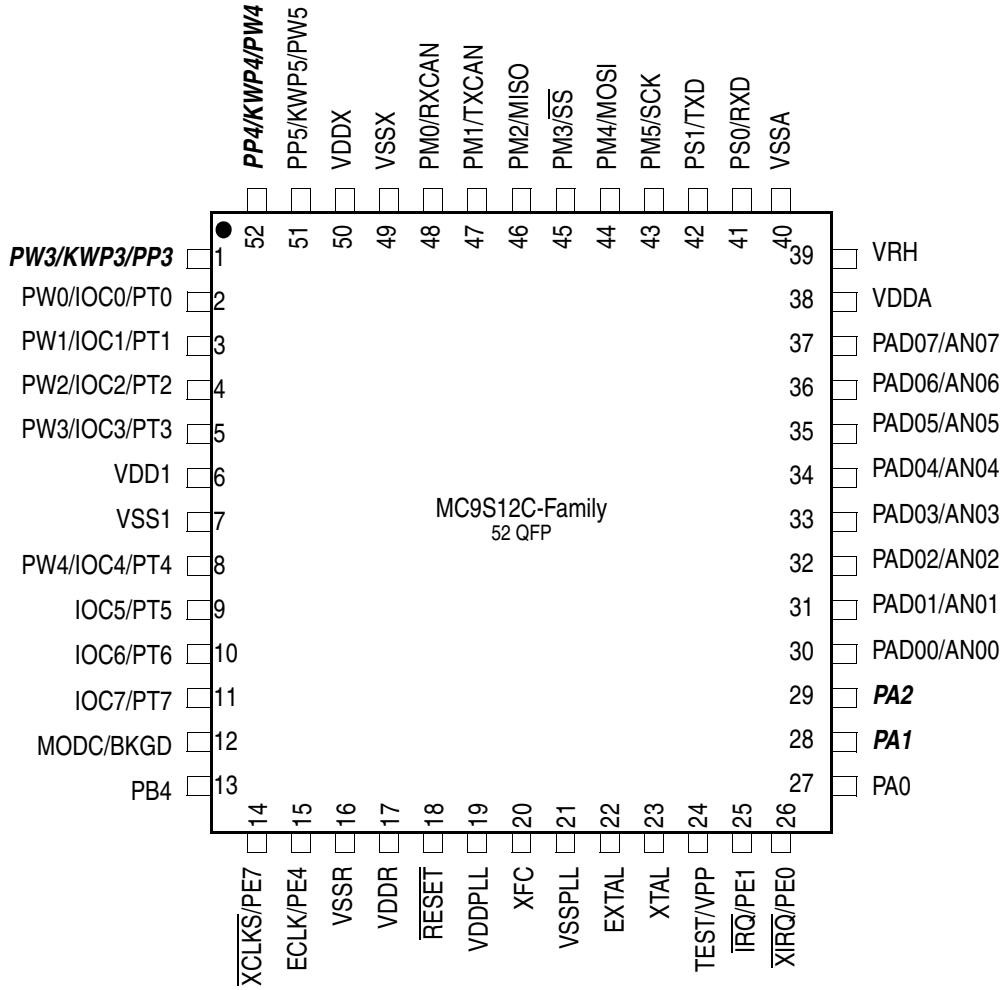
Figure 6 MCxS12C16 User Configurable Memory Map



Signals shown in **Bold** are not available on the 52 or 48 Pin Package
 Signals shown in **Bold Italic** are available in the 52, but not the 48 Pin Package

Figure 7 Pin Assignments in 80 QFP for MC9S12C-Family

!!! Pin-out is Subject to Change!!!



* Signals shown in **Bold** are not available on the 48 Pin Package

Figure 8 Pin assignments 52 QFP for MC9S12C-Family

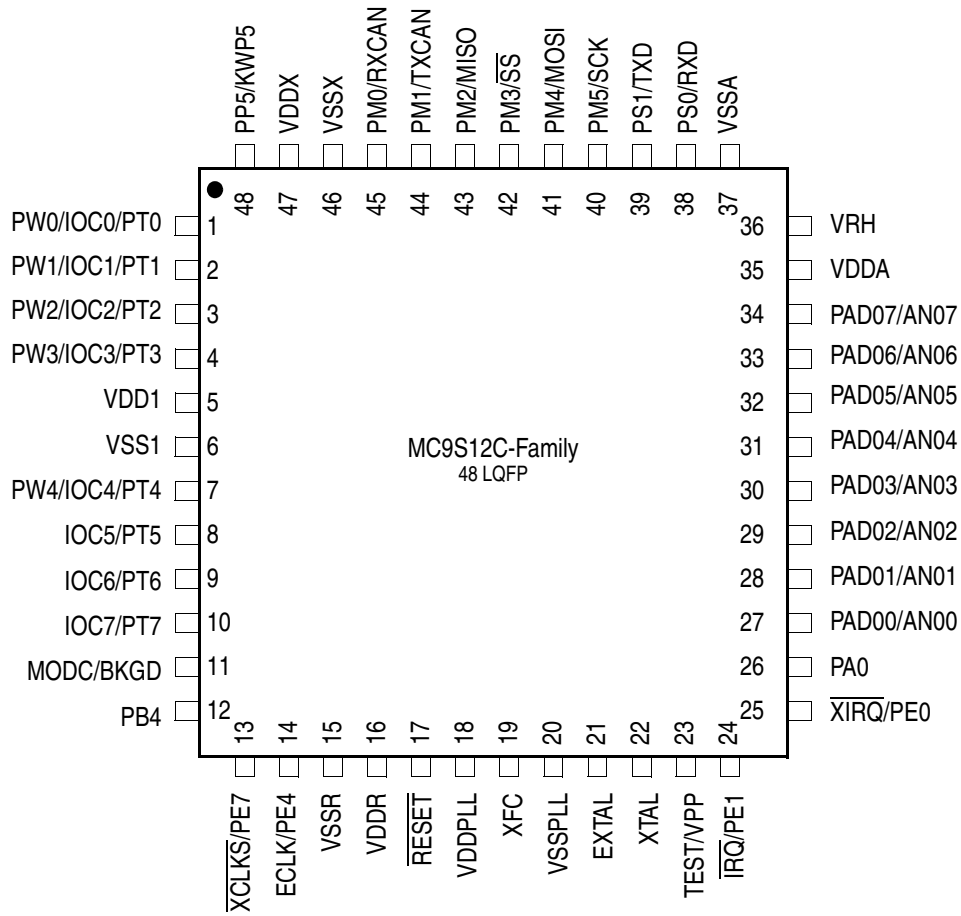
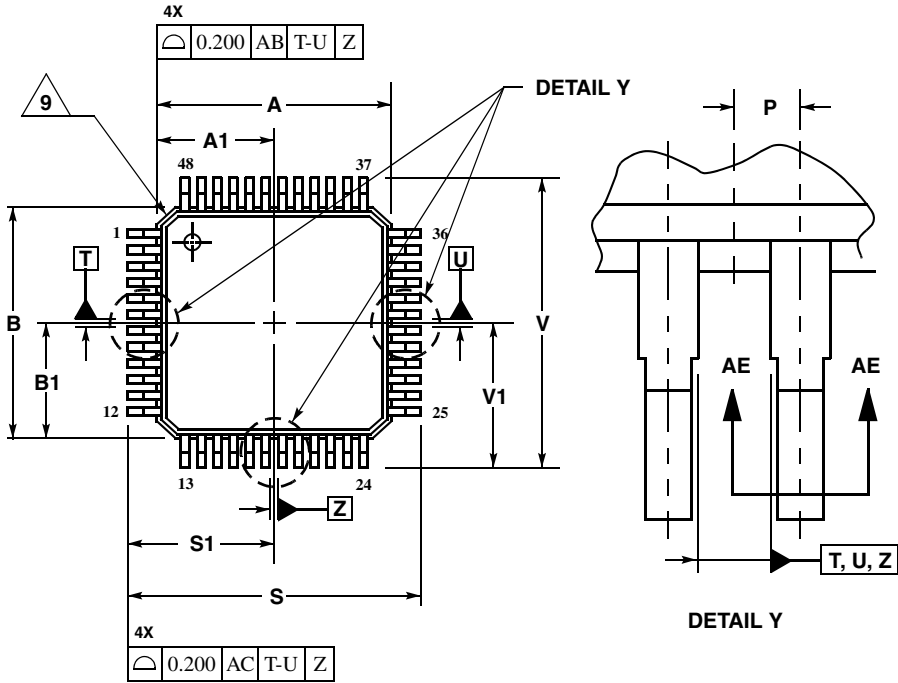


Figure 9 Pin Assignments in 48 LQFP for MC9S12C-Family

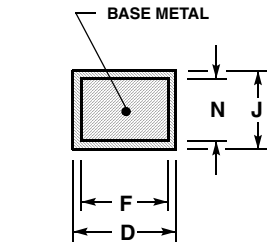
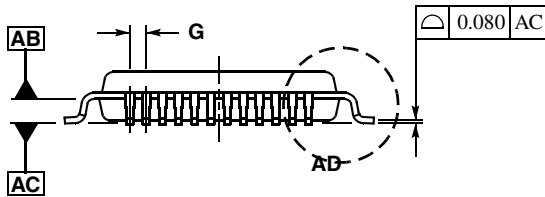
Package mechanical information



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
1. CONTROLLING DIMENSION: MILLIMETER.
2. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
3. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 7.000 BSC | |
| A1 | 3.500 BSC | |
| B | 7.000 BSC | |
| B1 | 3.500 BSC | |
| C | 1.400 | 1.600 |
| D | 0.170 | 0.270 |
| E | 1.350 | 1.450 |
| F | 0.170 | 0.230 |
| G | 0.500 BSC | |
| H | 0.050 | 0.150 |
| J | 0.090 | 0.200 |
| K | 0.500 | 0.700 |
| L | 0 ° | 7 ° |
| M | 12 ° REF | |
| N | 0.090 | 0.160 |
| P | 0.250 BSC | |
| R | 0.150 | 0.250 |
| S | 9.000 BSC | |
| S1 | 4.500 BSC | |
| V | 9.000 BSC | |
| V1 | 4.500 BSC | |
| W | 0.200 REF | |
| AA | 1.000 REF | |



SECTION AE-AE

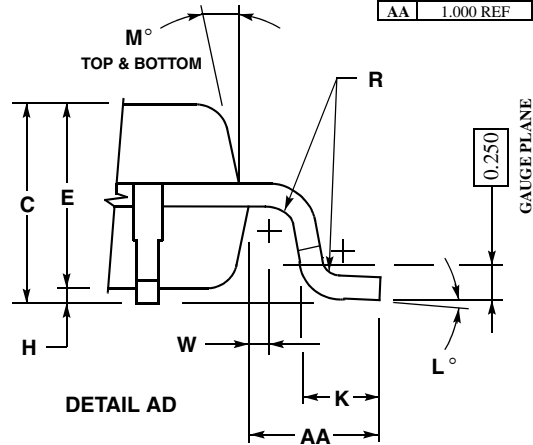
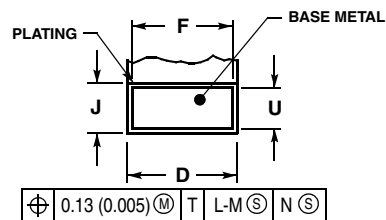
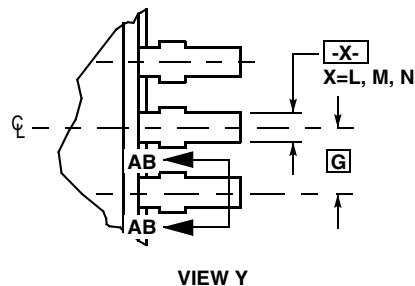
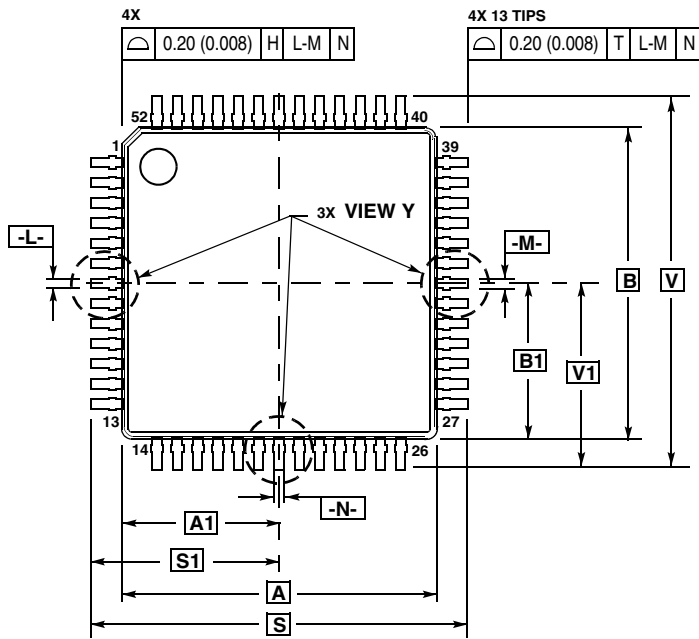


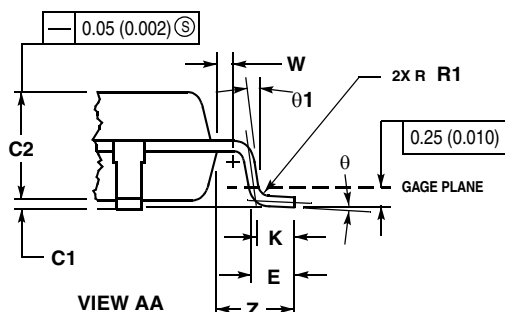
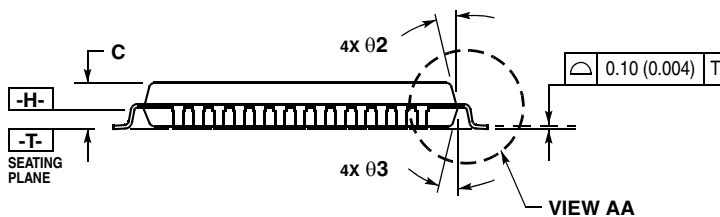
Figure 10 48-pin LQFP Mechanical Dimensions (case no.932-03 ISSUE F)



SECTION AB-AB
ROTATED 90° CLOCKWISE

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER
- DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
- DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND



| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 10.00 | BSC | 0.394 | BSC |
| A1 | 5.00 | BSC | 0.197 | BSC |
| B | 10.00 | BSC | 0.394 | BSC |
| B1 | 5.00 | BSC | 0.197 | BSC |
| C | --- | 1.70 | --- | 0.067 |
| C1 | 0.05 | 0.20 | 0.002 | 0.008 |
| C2 | 1.30 | 1.50 | 0.051 | 0.059 |
| D | 0.20 | 0.40 | 0.008 | 0.016 |
| E | 0.45 | 0.75 | 0.018 | 0.030 |
| F | 0.22 | 0.35 | 0.009 | 0.014 |
| G | 0.65 | BSC | 0.026 | BSC |
| J | 0.07 | 0.20 | 0.003 | 0.008 |
| K | 0.50 | REF | 0.020 | REF |
| R1 | 0.08 | 0.20 | 0.003 | 0.008 |
| S | 12.00 | BSC | 0.472 | BSC |
| S1 | 6.00 | BSC | 0.236 | BSC |
| U | 0.09 | 0.16 | 0.004 | 0.006 |
| V | 12.00 | BSC | 0.472 | BSC |
| V1 | 6.00 | BSC | 0.236 | BSC |
| W | 0.20 | REF | 0.008 | REF |
| Z | 1.00 | REF | 0.039 | REF |
| Ø | 0° | 7° | 0° | 7° |
| Ø1 | 0° | --- | 0° | --- |
| Ø2 | 12° | REF | 12° | REF |
| Ø3 | 12° | REF | 12° | REF |

Figure 11 52-pin LQFP Mechanical Dimensions (case no. 848D-03)

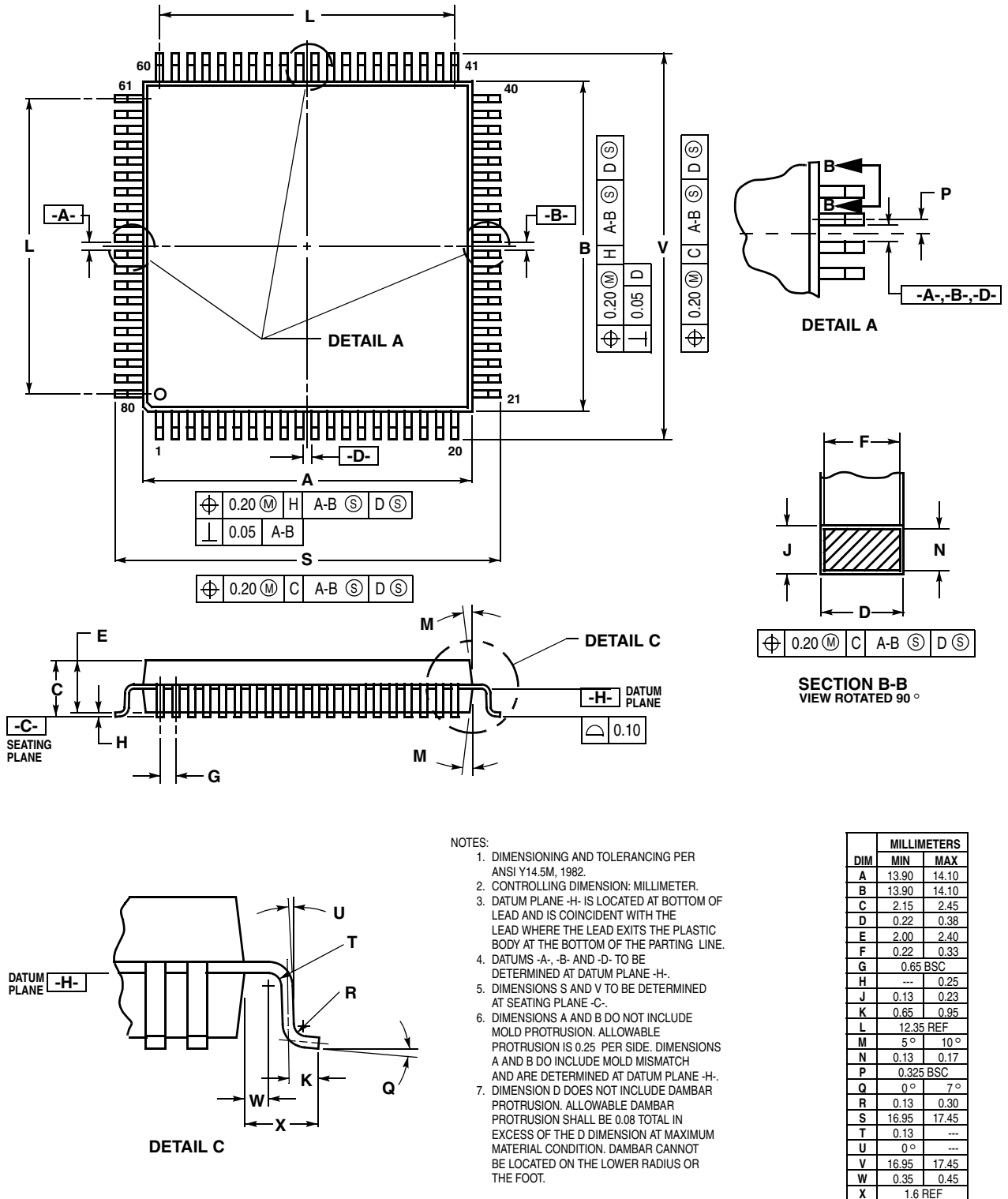



Figure 12 80-pin QFP Mechanical Dimensions (case no. 841B)

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140

HOME PAGE: <http://mcu.motps.com/>

JAPAN: Motorola Japan Ltd.; SPS, Technial Information Center, 3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573 Japan.
81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong. 852-266668334

CUSTOMER FOCUS CENTER: 1-800-521-6274

© Motorola, 2004



MOTOROLA More information on this product,
Go to: www.freescale.com