ECE331 Class Quiz 16 3 points maximum (Lecture 11 Microcontroller Interfacing)

Name: Solution CM Box: _____

1) Consider a 4-bit successive approximation analog-to-digital A/D converter (ADC), similar to the one on Slide #49:

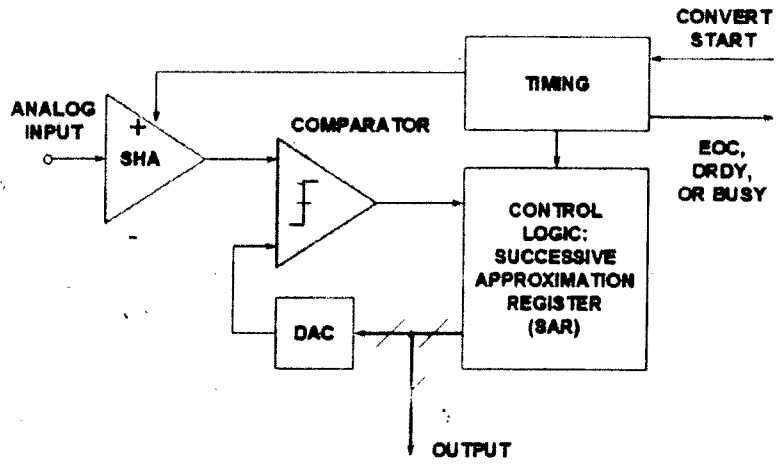
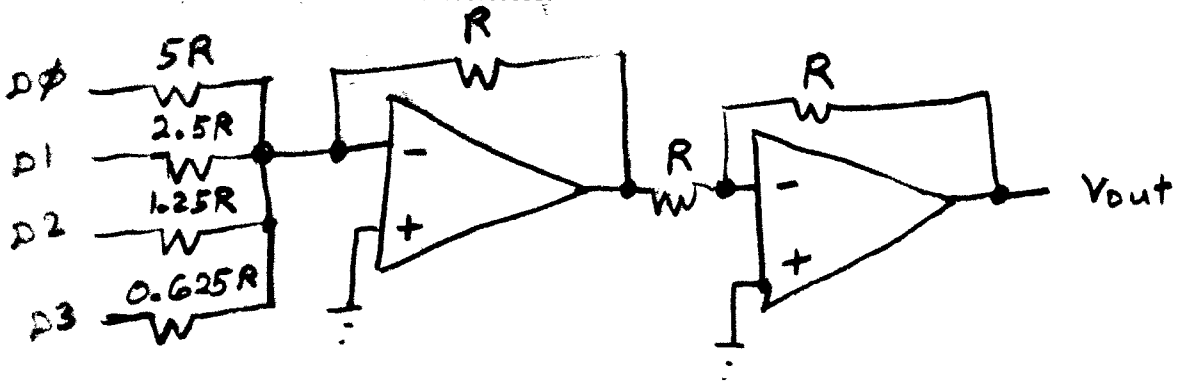


Figure 1: Basic Successive Approximation ADC

a) An ADC converter must contain a digital-to-analog converter (DAC). If a 4-bit DAC has a 0 to 15 V output range, then 0000 => 0 V, 0001 = 1 V, 11110 => 14 V, 1111 => 15 V. Assuming that a logic 1 input = 5 V and a logic 0 input = 0V, then design a 4-bit, 0 to 15 V DAC using two ideal OP AMPs and assorted resistors.



b) In a 4-bit successive approximation ADC shown in the diagram above, the analog input is successively approximated as a binary number, where the value of the MSB is first determined, then the next most significant bit, etc. Assume in our example that the analog input voltage is 10.3 V. This analog voltage value is held steady by the sample-and-hold amplifier (SHA) while the conversion process proceeds.

When a "Convert Start" pulse is received, the "timing" block generates 5 conversion clock pulses. During the first conversion clock pulse, the SHA goes from track to hold mode, the BUSY line is pulled high, and the successive approximation register (SAR) "tries out the MSB (Bit 3) for size" it does this by putting out 1000 as an input to the DAC. The comparator puts out "1", indicating

to the SAR control logic that the MSB of the converted number is indeed "1". So the "1" is retained in Bit 3 of the SAR through the rest of the conversion process.

During the second conversion clock pulse, the SAR tries out Bit 2 for size. The SAR outputs 1100 to the DAC. Now the comparator puts out 0, indicating to the SAR control logic that setting bit 2 to a 1 overshoots the mark. Therefore the "1" in this bit position is NOT retained.

During the third conversion clock pulse, the SAR tries out Bit 1 for size. The SAR outputs 1010 to the DAC. Now the comparator puts out 1, and the "1" in this bit position is retained.

During the fourth conversion clock pulse, the SAR tries out Bit 0 for size. The SAR outputs 1011 to the DAC. Now the comparator puts out 0, and the "1" in this bit position is not retained.

Now SAR = 1010

During the fifth and last conversion, the contents of the SAR holds the converted result, and this value is clocked into a output holding register (not shown above), whose outputs are driven through tristate drivers out of the data pins of the A/D converter onto an external computer data bus, assuming that this converter is like the converter shown on Slide #49. The BUSY line is pulled low to indicate the conversion is finished. Thus the previously converted result is held there until the computer reads from an address that asserts a tri-state enable pin that drives the data onto the bus. The conversion range of this converter could be changed from 0 to 15 V to 0 to 5 V by making what simple change in the DAC subcircuit? R → R/3. A 9-bit successive approximation converter with a 500 kHz conversion clock could perform a conversion in (10 clocks)(1/500 kHz) = 20 μs

2) In the multiplexed 8-digit 7-segment LED display circuit of Slide #56

a) The display is implemented with just 8 data output lines and 1 interrupt input.

b) What is the purpose of the 14528 one-shot monostable multivibrator?
Keep each LED lit for 1ms. Guards against LED segment overcurrent in event of software failure/debugging.

c) If each of the LED segments can take 10 mA average forward current, what is the maximum current pulse amplitude can be tolerated through each segment of these multiplexed displays?
≈ 10mA (8 digits) = 80mA current pulses (1/8 duty cycle)

d) What is the refresh rate of each segment in this display? $\frac{1}{8(1\text{ms})} = 125\text{Hz}$
How does this compare to the commonly-accepted persistence of vision rate? 30Hz (movie frame rate)

e) Keeping the 1-shot set to deliver a 1 ms pulse, what is the largest number of 7-seg digits that may be driven without falling below the commonly accepted persistence of vision rate?

$30\text{Hz} = \frac{1}{N(1\text{ms})} \Rightarrow N = \frac{1}{(30)(1\text{ms})} = 33.33$

⇒ 33 displays!

How many more output pins needed?
2 more outputs for 32 displays!