For a normally open SPST microswitch to exhibit the (often desirable) property of mechanical hysteresis means that:

As force on the open switch lever steadily increases, the switch suddenly closes at force F1, but then when force on the closed switch lever decreases, the switch suddenly opens at force F2. where

(a) F1 > F2 (b) F1 < F2 (c) F1 = F2 (d) F1 = F2 = 0

This property is desirable in applications where a clean and reliable switch closure is needed as a force slowly increases past a specific threshold, and the force is:

(a) changing fast

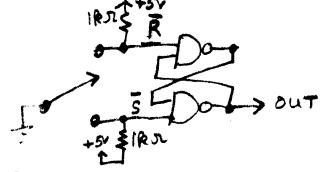
(b) shaky (jittery --- not smoothly increasing)

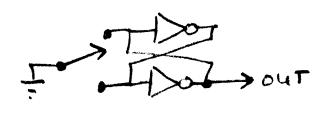
(c) very high

Show how to interconnect an SPDT switch (like the one on Slide #22) with two NAND gates and two resistors to generate a debounced switch output signal labeled "OUT". Hint: Recall that two NAND gates can be "cross-coupled" to form an SR latch with active low S and R inputs. Repeat using two invert gates, and an SPDT switch (resistor are not needed now).

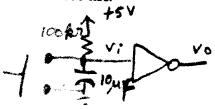
NAND Gate SPDT Switch Debounce Circuit

Invert Gate Switch Debounce Circuit





Assume that R1 = 100 k $\Omega$  and C1 = 10  $\mu F$  in the SPST switch debouncing circuit of Slide #24. Calculate the maximum allowable time between switch bounces as SW1 is depressed for the output "OUT" to remain high (and not bounce). Hint: recall the formula for the voltage across a capacitor in an RC circuit is: Vc(t) = Vf - (Vf-Vi)exp(-t/(RC)). Also recall that the input impedance of a CMOS gate such as the 74HC14 is much, much higher than 100 kΩ.



$$Y = RC = 100 \text{ A.s.} = 10 \text{ Indent higher than } V_c = 5 \text{ V} = 0 \text{ V}$$

$$V_c = 5 - 5 \text{ e}$$

$$2.5 \text{ V} = 5 - 5 \text{ e}$$

thousemax = - ln (1/2) = 0.693 s

Thounce\_max = 0.693.

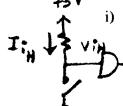
Note: This time is also the time you must wai to Low once #



Consider the following dc input specifications for the 74HCxx family of logic gates:

$$I_{IH}(max) = 10^{-6} \text{ A}$$
  $I_{IL}(max) = 10^{-6} \text{ A}$   $V_{IH}(min) = 3.15 \text{ V}$   $V_{IL}(max) = 1.35 \text{ V}$ 

a) Consider an SPST switch connected to the input of a 74HCxx gate between the gate input and ground, and a pullup resistor "Rpullup" connected between the gate input and Vcc = +5V.



i) Calculate the maximum permissible value of Rpullup.

ii) Calculate the dc power consumed in Rpullup (assuming the value calculated above) when the switch is closed.

iii) Calculate the dc power consumed in Rpullup when the switch is open.

$$\rho = (10^{-6})^2 (1.85 Mz) =$$

$$P_{HIGH} = 1.9 \mu W$$

b) Consider an SPST switch connected to the input a 74HCxx gate between the gate input and Vcc = 5V, and a pulldown resistor "Rpulldown" connected between the gate input and ground.

i) Calculate the maximum permissible value of Rpulldown.

ii) Calculate the dc power consumed in Rpulldown (assuming the value calculated above) when the switch is closed.

$$P_{Hi} = \frac{5^2}{RPA} = \frac{25 \text{ V}^2}{1.35 \text{ M} \text{ T}} = 18.5 \text{ MW}$$

iii) Calculate the dc power consumed in Rpull Strien the switch is open.

$$P_{LOW} = 1.4 u w$$

c) Which configuration (switch in pulldown path or switch in the pullup path has the slight advantage? Swin pulldown path



5) Will the magnetic reed switch of Slide #27 be most sensitive to a magnetic flux lines flowing



Consider the X-Y matrix keypad of Slide #30 which uses dedicated input and output ports.

a)	The diodes in the are used to protect the output port in the event of 2 keys in the same _? being pressed simultaneously.
	(a) row (b) column (c) row or column
b)	How many I/O pins would be required to scan a 25 key keypad?
c)	Instead of continuously scanning this keypad to see if a key is depressed, the software might write % 000000 to the output port and then wait for some value other than an % 1111 1111 to be read from the input port, indicating that a key has been depressed. However, once a key depression is detected, the scanning procedure described on this slide would have to be initiated to learn the identity of the depressed key. Assume that the MSB of both input and output ports are AT THE TOP of the respective port, that if the key in the 3 <sup>rd</sup> column from the left and the 6 <sup>th</sup> row from the top is depressed, then what binary scan code written to the output port will cause something other than \$FF to read from the input port? % 1111011. What binary value will be read from the input port when this occurs? % 1111011
d)	If the eight $10 \text{ k}\Omega$ pullup resistors are omitted in this circuit, while will the keyboard scanning circuit fail to work properly?
	(a) input lines may not read correctly (b) two key rollover detection will fail (c) the diodes will short out (d) the voltages at the output pins may be wrong