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S12VREGV1/D

VREG
Block User Guide
V01.01

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Motorola, Inc

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
0.1	2/21/01	2/21/01		VREG spec moved to SRS2.0 compliant format
1.0	4/05/01	4/05/01		Minor update, spec version number reflects clearcase label
V01.00	7/27/01	7/27/01		Document names have been added Names and Variable definitions have been hidden
V01.01	3/4/02	3/4/02		Changed Document Number

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Section 1 Introduction

1.1 Overview

The VREG block is used to generate the supply voltage (2.5V typ.) of the core logic and memory blocks out of the chip supply voltage (5V typ.).

1.2 Features

The block name includes these distinctive features:

- linear voltage regulator with two independent outputs
- power on reset signal generation

1.3 Modes of Operation

VREG can operate in three different modes

- RUN

  In run mode both regulating loops of the voltage regulator are active. This mode is selected whenever the CPU is neither in stop nor in pseudo stop mode and VREGEN is pulled high.

- STANDBY

  Standby mode is selected when the CPU is in stop or pseudo stop mode and VREGEN is pulled high. In standby mode the gates of the power transistors are directly connected to the reference voltage. In this case the voltage regulator acts as a voltage clamp. While in standby mode, the effective inner resistance of the regulator is increased, the quiescent current consumption of the regulator itself is heavily decreased.

- SHUTDOWN

  Shutdown mode is only available, when the device is equipped with a VREGEN bit. Shutdown mode is selected by tieing VREGEN to ground. In this case, the core logic must be supplied from external by applying 2.5V(+/-10%) on VDD and VDDPLL. The power on reset pulse generation circuit is not affected by selecting shutdown mode.

1.4 Block Diagram

Figure 1-1 is a block diagram of the VREG.

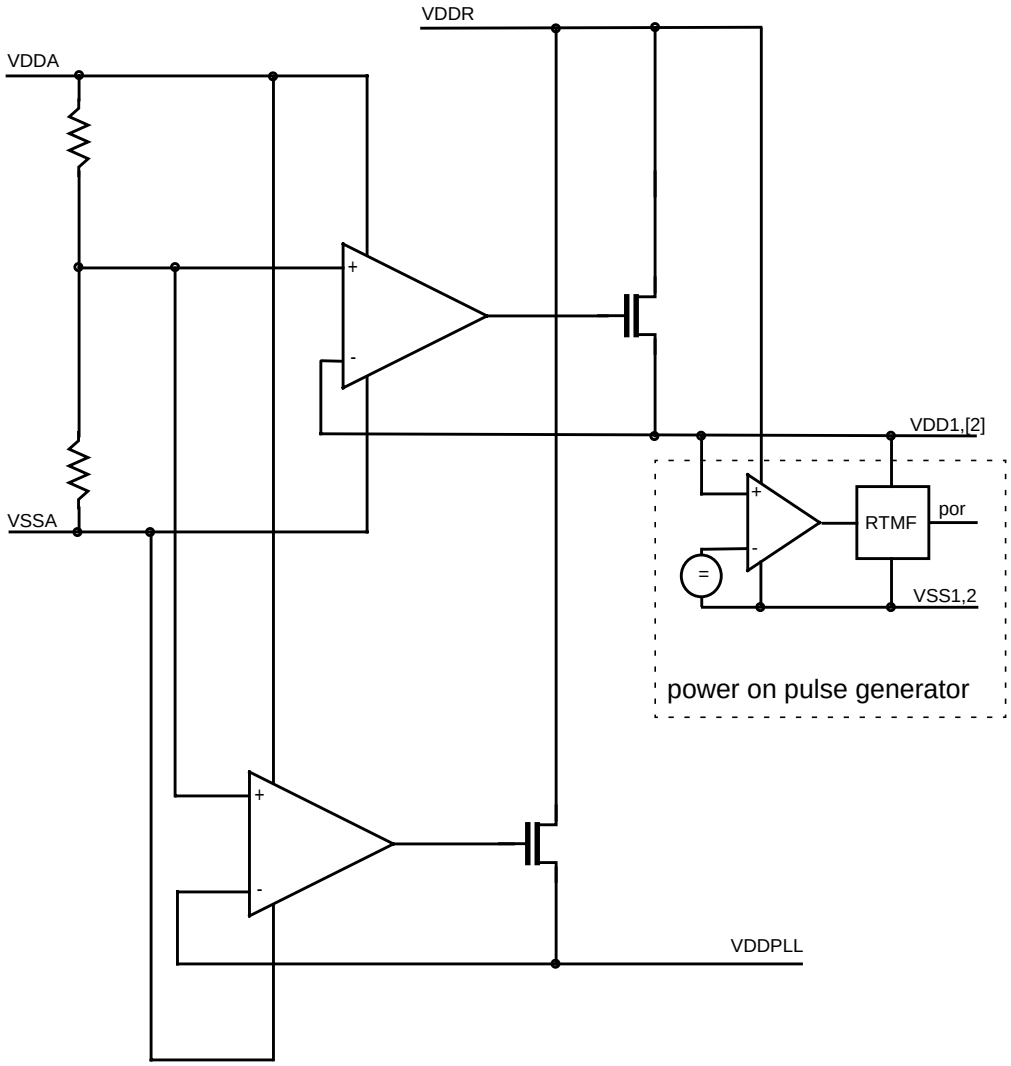

Figure 1-1 VREG Block Diagram

Section 2 Signal Description

2.1 Overview

Table 2-1 lists all pins associated with the VREG block.

Table 2-1 Signal Properties

Name	Function
VDDA	VREG positive reference and supply input
VSSA	VREG negative reference and supply input
VDDR	VREG power input
VDD1,[2]	VREG output 1st regulation loop
VSS1,[2]	VREG 1st regulation loop ground pin
VDDPLL	VREG output 2nd regulation loop
VSSPLL	VREG 2nd regulation loop ground pin
VREGEN	Selects Shutdown or Run/Standby mode

2.2 Detailed Signal Descriptions

2.2.1 VDDA, VSSA

VREG uses the VDDA/VSSA supply pin pair to supply the voltage regulator and to derive the reference voltage. The reference voltage VREG is regulating to is $(V_{DDA} - V_{SSA})/2$.

2.2.2 VDDR

VDDR is the power input to the voltage regulator. The output current of the two regulating loops is drawn out of this pin.

2.2.3 VDD1,[2], VSS1,[2]

VDD1, VSS1 and optional VDD2, VSS2 are the core logic supply pins. VDD1 and VDD2 are connected internally by metal as well as VSS1 and VSS2. Each power supply pin pair must be externally decoupled with a ceramic capacitor (100nF .. 220nF, X7R ceramic). VDD1,[2] is connected to the output of the first regulating loop of the voltage regulator.

2.2.4 VDDPLL, VSSPLL

VDDPLL and VSSPLL are the oscillator and pll supply pins. This supply pin pair must be externally decoupled with a ceramic capacitor (100nF .. 220nF, X7R ceramic). VDDPLL is connected to the output of the second regulating loop of the voltage regulator.

2.2.5 VREGEN

This optional pin is used to disable the voltage regulator if the core logic as well as the oscillators are supplied from external.

Section 3 Memory Map and Registers

3.1 Overview

The VREG block has no CPU accessible registers.

Section 4 Functional Description

4.1 General

The VREG block consists of a reference voltage generator, two operational amplifiers, two nmos power output stages and a power on reset pulse generation circuit.

4.1.1 Reference Generation

The reference generation is comprised of a resistor reference ladder between VDDA and VSSA. The output voltage of the reference ladder (V_{DDA} - V_{SSA})/2 is fed into both operational amplifiers as regulation reference.

4.1.2 Operational Amplifier

The operational amplifier compare the reference voltage ((V_{DDA} - V_{SSA})/2) with the actual output voltage (vdd or vddpll) to generate the gate voltage of the power output transistors.

In standby mode, the operational amplifiers are disabled and the gates of the power transistors are connected directly to the reference voltage in order to decrease the quiescent current.

4.1.3 Power Output Stage

Each power output stage consists of an nmos power transistor with its drain on VDDR and its source on VDD or VDDPLL.

4.1.4 Power On Reset Pulse Generation

A comparator monitors the actual value of VDD. If V_{DD} is below V_{POR}, the power on reset signal is asserted forcing the CPU in the power on reset state.

User Guide End Sheet

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