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Interrupt (INT) Module V1

HCS12 Microcontrollers

S12INTV1/D
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MOTOROLA.COM/SEMICONDUCTORS

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
1.02	5/1/2003	5/1/2003	John Langan	Creation of block user guide from core user guide version 1.5 (Oct. 12, 2001). Changes include: updating format and making end-customer friendly. Original release.

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Section 1 Introduction to Interrupt (INT)

This section describes the functionality of the Interrupt (INT) sub-block of the S12 Core Platform.

A block diagram of the Interrupt sub-block is shown in **Figure 1-1**.

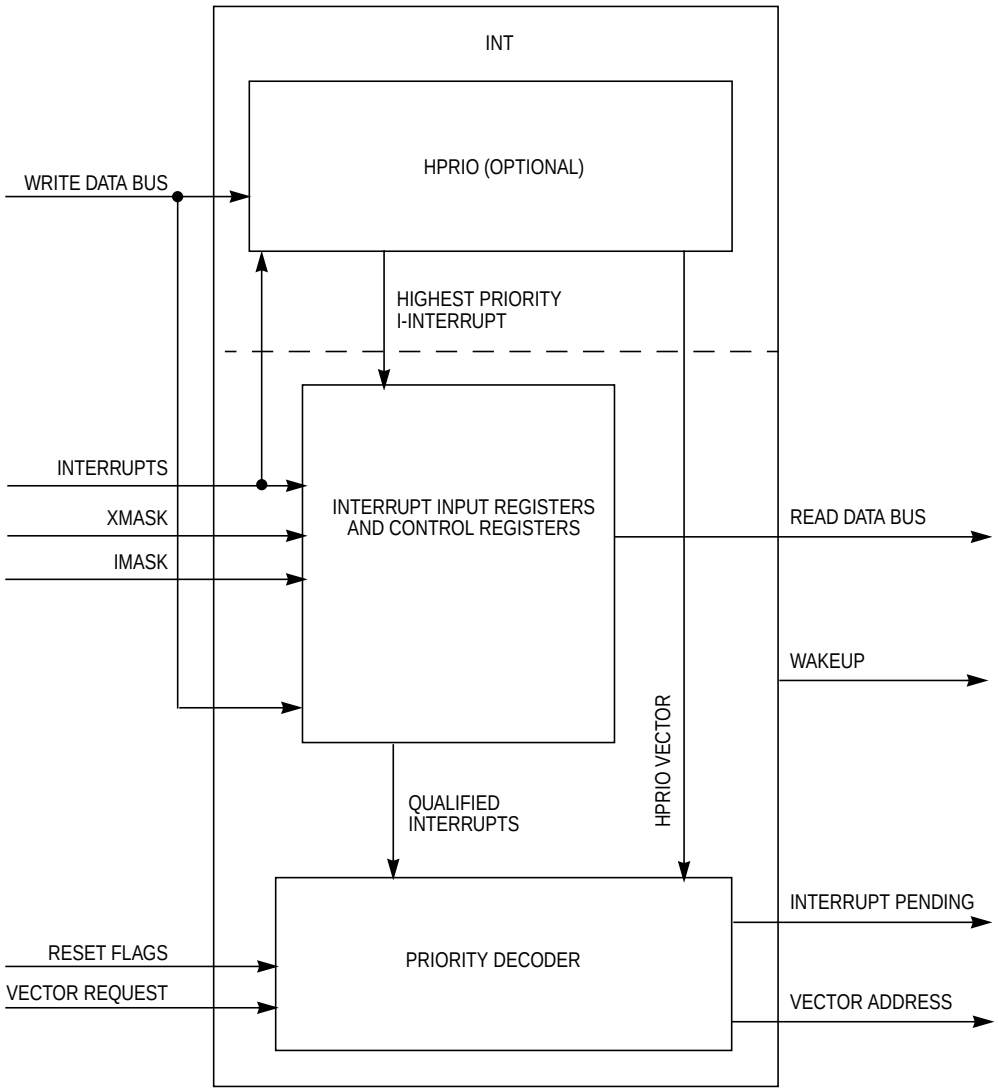

Figure 1-1 Interrupt Block Diagram

1.1 Overview

The Interrupt sub-block decodes the priority of all system exception requests and provides the applicable vector for processing the exception. The INT supports I-bit maskable and X-bit maskable interrupts, a nonmaskable Unimplemented Opcode Trap, a nonmaskable software interrupt (SWI) or Background Debug Mode request, and three system reset vector requests. All interrupt related exception requests are handled by the Interrupt sub-block (INT).

1.2 Features

The INT includes these features:

- Provides two to 122 I-bit maskable interrupt vectors ($FF00–$FFF2)
- Provides one X-bit maskable interrupt vector ($FFF4)
- Provides a nonmaskable software interrupt (SWI) or Background Debug Mode request vector ($FFF6)
- Provides a nonmaskable Unimplemented Opcode Trap (TRAP) vector ($FFF8)
- Provides three system reset vectors ($FFFA–$FFFE) (Reset, CMR, and COP)
- Determines the appropriate vector and drives it onto the address bus at the appropriate time
- Signals the CPU that interrupts are pending
- Provides control registers which allow testing of interrupts
- Provides additional input signals which prevents requests for servicing I and X interrupts
- Wakes the system from stop or wait mode when an appropriate interrupt occurs or whenever $\overline{\text{XIRQ}}$ is active, even if $\overline{\text{XIRQ}}$ is masked
- Provides asynchronous path for all I and X interrupts, ($FF00–$FFF4)
- (Optional) Selects and stores the highest priority I interrupt based on the value written into the HPRIO register

1.3 Modes of Operation

The functionality of the INT sub-block in various modes of operation is discussed in the subsections that follow.

1.3.1 Normal Operation

The INT operates the same in all normal modes of operation.

1.3.2 Special Operation

Interrupts may be tested in special modes through the use of the interrupt test registers.

1.3.3 Emulation Modes

The INT operates the same in emulation modes as in normal modes.

1.4 Low-Power Options

The INT does not contain any user-controlled options for reducing power consumption. The operation of the INT in low-power modes is discussed in the following subsections.

1.4.1 Run Mode

The INT does not contain any options for reducing power in run mode.

1.4.2 Wait Mode

Clocks to the INT can be shut off during system wait mode and the asynchronous interrupt path will be used to generate the wake-up signal upon recognition of a valid interrupt or any $\overline{\text{XIRQ}}$ request.

1.4.3 Stop Mode

Clocks to the INT can be shut off during system stop mode and the asynchronous interrupt path will be used to generate the wake-up signal upon recognition of a valid interrupt or any $\overline{\text{XIRQ}}$ request.

Section 2 External Signal Description

Most interfacing with the Interrupt sub-block is done within the Core. However, the Interrupt does receive direct input from the Multiplexed External Bus Interface (MEBI) sub-block of the Core for the $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$ pin data.

Section 3 Memory Map/Register Definition

A summary of the registers associated with the Interrupt sub-block is shown in **Figure 3-1**. Detailed descriptions of the registers and associated bits are given in the subsections that follow.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
$0015	ITCR	Read	0	0	0	WRTINT	ADR3	ADR2	ADR1	ADR0
		Write								
$0016	ITEST	Read	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write								
$001F	HPRIO	Read	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write								

= Unimplemented

Figure 3-1 Interrupt Register Summary

3.1 Interrupt Test Control Register

Register address: Base + $0015

	7	6	5	4	3	2	1	0
R	0	0	0	WRTINT	ADR3	ADR2	ADR1	ADR0
W								
Reset:	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 3-2 Interrupt Test Control Register (ITCR)

Read: see individual bit descriptions

Write: see individual bit descriptions

WRTINT — Write to the Interrupt Test Registers

Read: anytime

Write: only in special modes and with I-bit mask and X-bit mask set.

1 = Disconnect the interrupt inputs from the priority decoder and use the values written into the ITEST registers instead.

0 = Disables writes to the test registers; reads of the test registers will return the state of the interrupt inputs.

NOTE: *Any interrupts which are pending at the time that WRTINT is set will remain until they are overwritten.*

ADR3–ADR0 — Test Register Select Bits

Read: anytime

Write: anytime

These bits determine which test register is selected on a read or write. The hexadecimal value written here will be the same as the upper nibble of the lower byte of the vector selects. That is, an “F” written into ADR3–ADR0 will select vectors $FFFE–$FFF0 while a “7” written to ADR3–ADR0 will select vectors $FF7E–$FF70.

3.2 Interrupt Test Registers

Register address: Base + $0016

	7	6	5	4	3	2	1	0
R W	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
Reset:	0	0	0	0	0	0	0	0

Figure 3-3 Interrupt TEST Registers (ITEST)

Read: Only in special modes. Reads will return either the state of the interrupt inputs of the Interrupt sub-block (WRTINT = 0) or the values written into the TEST registers (WRTINT = 1). Reads will always return zeroes in normal modes.

Write: Only in special modes and with WRTINT = 1 and CCR I mask = 1.

INTE–INT0 — Interrupt TEST Bits

These registers are used in special modes for testing the interrupt logic and priority independent of the system configuration. Each bit is used to force a specific interrupt vector by writing it to a logic one state. Bits are named INTE through INT0 to indicate vectors $FFxE through $FFx0. These bits can be written only in special modes and only with the WRTINT bit set (logic one) in the Interrupt Test Control Register (ITCR). In addition, I interrupts must be masked using the I bit in the CCR. In this

state, the interrupt input lines to the Interrupt sub-block will be disconnected and interrupt requests will be generated only by this register. These bits can also be read in special modes to view that an interrupt requested by a system block (such as a peripheral block) has reached the INT module.

There is a test register implemented for every 8 interrupts in the overall system. All of the test registers share the same address and are individually selected using the value stored in the ADR3–ADR0 bits of the Interrupt Test Control Register (ITCR).

NOTE: *When ADR3–ADR0 have the value of $F, only bits 2–0 in the ITEST register will be accessible. That is, vectors higher than $FFF4 cannot be tested using the test registers and bits 7–3 will always read as a logic zero. If ADR3–ADR0 point to an unimplemented test register, writes will have no effect and reads will always return a logic zero value.*

3.3 Highest Priority I Interrupt (Optional)

Register address: Base + $001F

	7	6	5	4	3	2	1	0
R	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
W								
Reseet:	1	1	1	1	0	0	1	0

= Unimplemented or Reserved

Figure 3-4 Highest Priority I Interrupt Register (HPRIO)

Read: anytime

Write: only if I mask in CCR = 1

PSEL7–PSEL1 — Highest Priority I Interrupt Select Bits

The state of these bits determines which I-bit maskable interrupt will be promoted to highest priority (of the I-bit maskable interrupts). To promote an interrupt, the user writes the least significant byte of the associated interrupt vector address to this register. If an unimplemented vector address or a non I-bit masked vector address (value higher than $F2) is written, IRQ ($FFF2) will be the default highest priority interrupt.

Section 4 Functional Description

The Interrupt sub-block processes all exception requests made by the CPU. These exceptions include interrupt vector requests and reset vector requests. Each of these exception types and their overall priority level is discussed in the subsections below.

4.1 Interrupt Exception Requests

As shown in the block diagram in **Figure 1-1**, the INT contains a register block to provide interrupt status and control, an optional Highest Priority I Interrupt (HPRIO) block, and a priority decoder to evaluate whether pending interrupts are valid and assess their priority.

4.1.1 Interrupt Registers

The INT registers are accessible only in special modes of operation and function as described in **3.1 Interrupt Test Control Register** and **3.2 Interrupt Test Registers** previously.

4.1.2 Highest Priority I-Bit Maskable Interrupt

When the optional HPRIO block is implemented, the user is allowed to promote a single I-bit maskable interrupt to be the highest priority I interrupt. The HPRIO evaluates all interrupt exception requests and passes the HPRIO vector to the priority decoder if the highest priority I interrupt is active. RTI replaces the promoted interrupt source.

4.1.3 Interrupt Priority Decoder

The priority decoder evaluates all interrupts pending and determines their validity and priority. When the CPU requests an interrupt vector, the decoder will provide the vector for the highest priority interrupt request. Because the vector is not supplied until the CPU requests it, it is possible that a higher priority interrupt request could override the original exception that caused the CPU to request the vector. In this case, the CPU will receive the highest priority vector and the system will process this exception instead of the original request.

NOTE: *Care must be taken to ensure that all exception requests remain active until the system begins execution of the applicable service routine; otherwise, the exception request may not get processed.*

If for any reason the interrupt source is unknown (e.g., an interrupt request becomes inactive after the interrupt has been recognized but prior to the vector request), the vector address will default to that of the last valid interrupt that existed during the particular interrupt sequence. If the CPU requests an interrupt vector when there has never been a pending interrupt request, the INT will provide the Software Interrupt (SWI) vector address.

4.2 Reset Exception Requests

The INT supports three system reset exception request types: normal system reset or power-on-reset request, Crystal Monitor reset request, and COP Watchdog reset request. The type of reset exception request must be decoded by the system and the proper request made to the Core. The INT will then provide the service routine address for the type of reset requested.

4.3 Exception Priority

The priority (from highest to lowest) and address of all exception vectors issued by the INT upon request by the CPU is shown in **Table 4-1**.

Table 4-1 Exception Vector Map and Priority

Vector Address	Source
$FFFE–$FFFF	System reset
$FFFC–$FFFD	Crystal monitor reset
$FFFA–$FFFB	COP reset
$FFF8–$FFF9	Unimplemented opcode trap
$FFF6–$FFF7	Software interrupt instruction (SWI) or BDM vector request
$FFF4–$FFF5	$\overline{\text{XIRQ}}$ signal
$FFF2–$FFF3	$\overline{\text{IRQ}}$ signal
$FFF0–$FF00	Device-specific I-bit maskable interrupt sources (priority in descending order)

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