RTL8201

Single port 10/100Mbps Fast Ethernet Phyceiver

1. Features

Realtek's RTL8201 is a Fast Ethernet Phyceiver with MII interface to MAC chip. It provides the following features:

- Support MII interface
- Support 10/100Mbps operation
- Support half/full duplex operation
- IEEE 802.3/802.3u compliant
- Support IEEE 802.3u clause 28 auto negotiation
- Support power down mode
- Support Link Down Power Saving mode operation.
- Support repeater mode
- Speed/duplex/auto negotiation adjustable
- 3.3V operation with 5V signal tolerance
- Low operation power consumption
- Adaptive Equalization
- 25Mhz crystal/oscillator as clock source
- Many LEDs support to indicate network status
- Support 7-wire SNI (Serial Network Interface) interface.
- Flow control ability support to co-work with MAC(by MDC/MDIO)
- 48 pin LQFP package

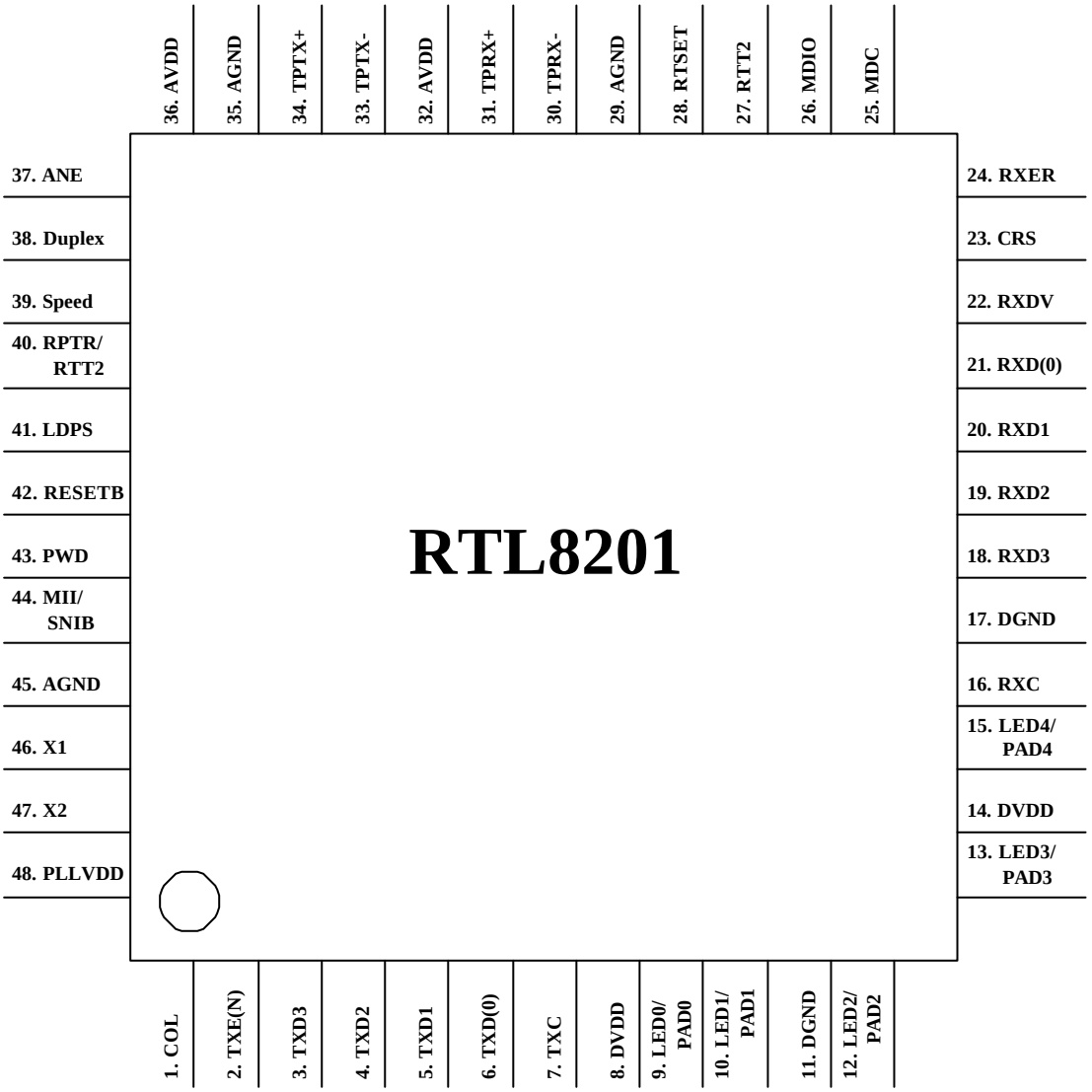
Applications:

Network Interface Adapter, MAU, CNR, ACR, Ethernet Hub, Ethernet Switch, or any embedded system with Ethernet MAC that need twist pair physical connection.

2. General Description

The RTL8201 is a single-port Phyceiver with MII(Media Independent Interface) that implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer(PCS), Physical Medium Attachment(PMA), Twisted Pair Physical Medium Dependent Sublayer(TP-PMD), 10Base-Tx Encoder/Decoder and Twisted Pair Media Access Unit(TPMAU). And it is fabricated with an advanced CMOS process to meet low voltage and low power requirement.

3. Pin Assignment



4. Pin Descriptions

4.1 100 Mbps MII & PCS Interface

Symbol	Type	Pin(s) No.	Description
TXC	O	7	Transmit Clock: This pin provides a continuous clock as a timing reference for TXD[3:0] and TXEN.
TXEN	I	2	Transmit Enable: The input signal indicates the presence of a valid nibble data on TXD[3:0].
TXD[3:0]	I	3, 4, 5, 6	Transmit Data: MAC will source TXD[0..3] synchronous with TXC when TXEN is asserted.
RXC	O	16	Receive Clock: This pin provides a continuous clock reference for RXDV and RXD[0..3] signals. RXC is 25MHz in the 100Mbps mode and 2.5Mhz in the 10Mbps mode.
COL	O	1	Collision Detected: COL is asserted high when a collision is detected on the media.
CRS	I/O	23	Carrier Sense: This pin's signal is asserted high if the media is not in IDEL state.
RXDV	O	22	Receive Data Valid: This pin's signal is asserted high when received data is present on the RXD[3:0] lines; the signal is deasserted at the end of the packet. The signal is valid on the rising of the RXC.
RXD[3:0]	O	18, 19, 20, 21	Receive Data: These are the four parallel receive data lines aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY).
RXER	O	24	Receive error: if any 5B decode error occurred such as invalid J/K, T/R, invalid symbol, this pin will go high
MDC	I	25	Management Data Clock: This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks.
MDIO	I/O	26	Management Data Input/Output: This pin provides the bi-directional signal used to transfer management information.

4.2 SNI (Serial Network Interface): 10Mbps only

Symbol	Type	Pin(s) No.	Description
COL	O	1	Collision Detect
RXD	O	21	Received Serial Data
CRS	O	23	Carry Sense
RXC	O	16	Receive Clock: resolved from received data
TXD	I	6	Transmit Serial Data
TXC	O	7	Transmit Clock: generate by PHY
TXE	I	2	Transmit Enable: for MAC to indicate transmit operation

4.3 Clock Interface

Symbol	Type	Pin(s) No.	Description
X2	O	47	25Mhz Crystal Output: This pin provides the 25MHz crystal output.
X1	I	46	25Mhz Crystal Input: This pin provides the 25MHz crystal input.

4.4 100Mbps Network Interface

Symbol	Type	Pin(s) No.	Description
TPTX+ TPTX-	O O	34 33	Transmit Output
RTSET	I	28	Transmit bias resistor connection, should pull to GND by a 1.69K resistor.
TPRX+ TPRX-	I I	31 30	Receive input

4.5 Device Configuration Interface

Symbol	Type	Pin(s) No.	Description
PWD	I	43	Set high to put RTL8201 into Power Down mode
RPTR/RTT2	I	40	Set high to put RTL8201 into repeater mode. In test mode, this pin is re-defined as RTT2.
SPEED	I	39	Set high to put RTL8201 into force 10Mbps operation
DUPLEX	I	38	Set high to enable full duplex
ANE	I	37	Set high to enable Autonegotiate mode, set low to force mode
LDPS	I	41	Set high to put RTL8201 into LDPS mode,

MII/SNIB/ TXD5(test)	I	44	Pull high to set RTL8201 into MII mode operation

4.6 LED Interface/PHY Address Config

Symbol	Type	Pin(s) No.	Description
LED0/ PAD0	O	9	Link LED
LED1/ PAD1	O	10	Full Duplex LED
LED2/ PAD2	O	12	Link 100/ACT LED
LED3/ PAD3	O	13	Link 10/ACT LED
LED4/ PAD4	O	15	Collision LED

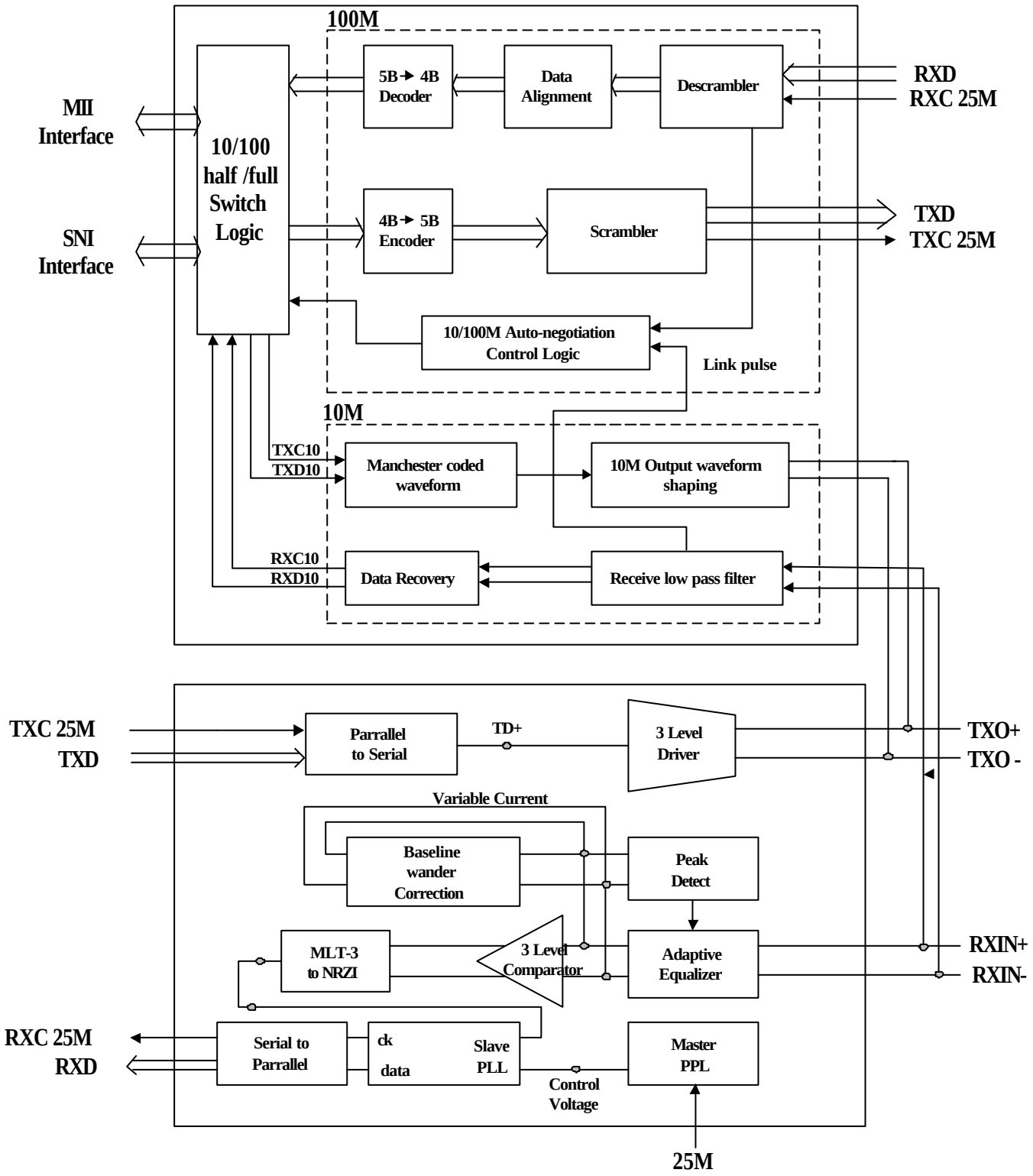
4.7 Reset and Test pin

Symbol	Type	Pin(s) No.	Description
RTT2	I	27	Test pin
RESETB	I	42	RESETB: Setting low to reset the chip.

4.8 Power and Ground pin

Symbol	Type	Pin(s) No.	Description
PLLVDD	P	48	3.3V power supply for PLL, should be well decoupled and use a bead with 100ohm @ 100Mhz to connect to analog power
AVDD	P	32,36	3.3V power supply for analog circuit, should be well decoupled
AGND	P	29,35,45	Analog Ground, should be connected to a larger GND plane
DVDD	P	8,14	Digital Power, 3.3V power supply for digital circuit.
DGND	P	11,17	Digital Ground, should be connected to a larger GND plane

5. Functional Block Diagram



6. Functional Description

The RTL8201 Phyceiver is a physical layer device that integrates 10 Base T and 100 Base TX functions and some extra power manage features into a 48 pin single chip that is used in 10/100 Fast Ethernet application. This device supports the following function:

- MII interface with MDC/MDIO management interface to communicate with MAC
- IEEE 802.3u clause 28 Auto-Negotiation ability
- Flow control ability support to cooperate with MAC
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO.
- Flexible LED configuration.
- 7-wire SNI(Serial Network Interface) support, works only on 10Mbps mode.
- 4B/5B transform
- Scrambling/ De-scrambling
- NRZ to NRZI, NRZI to MLT3
- Manchester Encode and Decode for 10 BaseT operation
- Clock and Data recovery
- Adaptive Equalization
- Power Down mode support

6.1 MII and management interface

To set up RTL8201 for MII mode operation, pull MII/SNIB pin high and properly set up the ANE, SPEED, and DUPLEX pins.

The MII(Media Independent Interface) is a 18-signals interface which is described in IEEE 802.3u supplying a standard interface between PHY and MAC layer. This interface operates in two frequencies – 25Mhz and 2.5Mhz to support 100Mbps/10Mbps bandwidth for both transmit and receive function. While transmitting packet, the MAC will first assert TXEN signal and change byte data into 4 bits nibble and pass to the PHY by TXD[0..3]. PHY will sample TXD[0..] synchronously with TXC —the transmit clock signal supply by PHY – during the interval TXEN is asserted. While receiving packet, the PHY will assert the RXEN signal, pass the received nibble data RXD[0..3] clocked by RXC, which is recovered from the received data. CRS and COL signals are used for collision detection and handling.

MAC layer device can control PHY by MDC/MDIO management interface, but for properly operation, the PHY address need to be well configured so the management command can be delivered to the PHY. MDC can be software generated to clock the 1 bit serial data stream into/from MDIO to access the PHY' s registers.

In 100Base TX mode, when decoded signal in 5B is not IDLE, CRS signal will assert and when 5B is recognized as IDLE it will be de-asserted. In 10BaseT mode, CRS will assert when the 10M preamble been confirmed and will be de-asserted when IDLE pattern been confirmed.

The RXDV signal will be asserted when decoded 5B are /J/K/ and will be deasserted if the 5B are /T/R/ or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as CRS signal.

6.2 Media Interface

100BAse Tx/Rx

Transmit function is performed as follow:

First the transmit 4 bits nibbles (TXD[0..3]) clocked in 25Mhz(TXC) will be transform into 5B symbol code so called 4B/5B encode, then scrambling, serializing and converting to 125Mhz, and NRZ to NRZI. After this process, the NRZI signal will pass to the MLT3 encoder, then to the transmit line driver. The transmitter will first assert TXEN. Before transmitting the data pattern, it will first send a /J/K/ symbol(Start-of-frame delimiter), then the data symbol and finally add a /T/R/ symbol known as End-of-frame delimiter. The 4B/5B and the scramble process can bypass by setting the PHY register. For better EMI performance consideration, the seed of the scrambler is related to the PHY address, so in hub/switch environment, every RTL8201 will be set into different PHY address so they will use different scrambler seed, this will spread the output MLT3 signals.

Receive function is performed as follow:

the received signal will first be compensate by adaptive equalizer to make up with the signal loss due to cable attenuation and ISI. Then Baseline wander corrector will monitor the process and dynamically apply to the process of signal equalization. Then PLL will recover the timing information from the signals and form the receive clock, by this, the received signal may sample to form NRZI data, then NRZI to NRZ process, unscramble the data, serial to parallel, 5B to 4B then pass the 4B nibble to the MII interface.

RTL8201 will not use TXER signal

6.3 Auto-negotiation and Parallel Detection

RTL8201 supports IEEE 802.3u clause 28 Auto-negotiation operation that can cooperate with other transceiver supporting auto-negotiation. By this mechanic, RTL8201 can auto detect the link partner's ability and decide the highest speed/duplex configuration and transmit/receive in this configuration. If the link partner do not support Auto-negotiation, then RTL8201 will suppose to be half duplex and enter the parallel detection. So RTL8201 will default transmit FLP and waiting for the link partner to response. If RTL8201 receive FPL, then auto-negotiation process will go on. If it received NLP, then RTL8201 will change to 10Mbps and half duplex mode. If it received 100Mbps IDLE pattern, it will change to 100Mbps and half duplex mode.

To enable auto-negotiation mode operation, pull ANE pin high and the SPEED pin and DUX pin will set up the ability of RTL8201. The auto-negotiation mode can be external disable by pull ANE pin low and in this case, SPEED pin and DUX pin will change the media configuration of RTL8201.

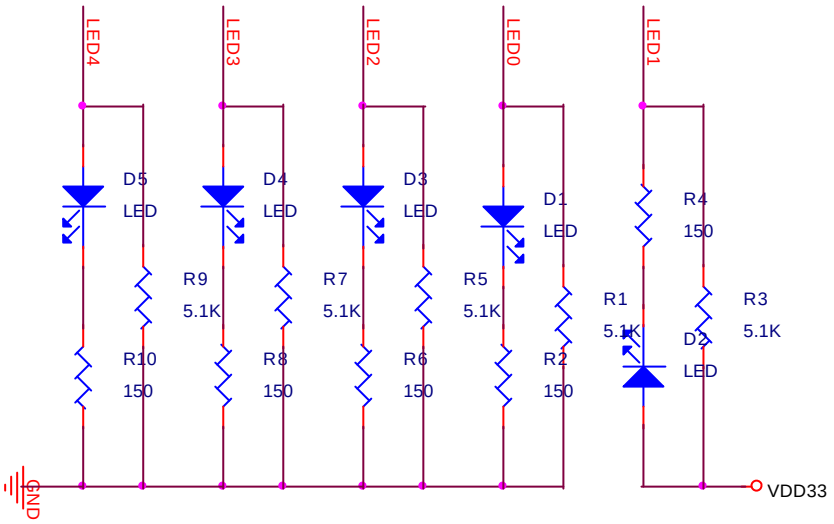
Below are a list for all configurations of ANE/SPEED/DUX pins and its operation mode.

ANE	SPEED	DUX	operation
H	L	L	Auto-negotiation enable, the ability filed doesn't support 100Mbps and full duplex mode operation
H	L	H	Auto-negotiation enable, the ability filed doesn't support 100Mbps operation
H	H	L	Auto-negotiation enable, the ability filed doesn't support full duplex mode operation
H	H	H	Default setup, auto-negotiation enable, the RTL8201 will support 10BaseT /100BaseTX, half/full duplex mode operation
L	L	L	Auto-negotiation disable, force RTL8201 in 10BaseT and half duplex mode
L	L	H	Auto-negotiation disable, force RTL8201 in 10BaseT and full duplex mode
L	H	L	Auto-negotiation disable, force RTL8201 in 100BaseTX and half duplex mode
L	H	H	Auto-negotiation disable, force RTL8201 in 100BaseTX and full duplex mode

6.4 LED and PHY address configure

The LED pins are duplexed with PHY address pin, since the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED

usage must be considered in order to avoid contention. Specially, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/rest. For example, if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver.



Above is an example of LED and PHY address config. In this design, the PHY address had been set to (00010b), i.e., (02h). And all useable LED had been connected. You can remove some LED in your design.

The LED define and the meanings is listed as below:

LED0	Link
LED1	Full Duplex
LED2	Link 10-Activity
LED3	Link 100-Activity
LED4	Collision

6.5 Hardware configure and auto-negotiate ability setting

1) **PWD pin**: pull high to Power Down RTL8201, default pulls low. Please refer to section 6.6: Power Down mode and Link Down Power Saving.
2) **RPTR pin**: pull high to set RTL8201 to repeater mode, default pulls low. Please refer to section 6.7: Repeater mode operation.

3) **LDPS pin**: pull high to set RTL8201 in LDPS mode, default pulls low. Please refer to section 6.6: Power Down mode and Link Down Power Saving.
4) **MII/SNIB**: pull high to set RTL8201 into MII mode operation, it is the default mode RTL8201 working. Pull low this pin will set RTL8201 into SNI mode operation, when setting to SNI mode, RTL8201 will works on 10Mbps. Please refer to Section 6.9 for more detail information.
5) **ANE pin**: pull high to enable Auto-negotiation (default), pull low to disable and parallel detection mechanic will active. Please refer to section 6.3:Autonegociation and Parallel Detection
6) **Speed pin**: When ANE pull high, this will setup the ability. When ANE pull low, pull low to force to 10Mbps and pull high to force 100Mbps operation. Please refer to section 6.3: Auto-negotiation and Parallel Detection
7) **DUX pin**: When ANE pull high, this will setup the ability. When ANE pull low, pull low to force to half duplex and pull high to force full duplex operation. Please refer to section 6.3: Auto-negotiation and Parallel Detection.

6.6 Power Down mode and Link Down Power Saving

RTL8201 supplies 4 kinds of Power Saving mode operation:

1) **Analog off**: set 1 to bit 11 of register 17 will put RTL8201 into analog off state. In analog off state, RTL8201 will power down all analog functions such as transmit, receive, PLL, etc except internal 25Mhz crystal oscillator. The digital functions in this mode are still available so you can set it back to re-acquire analog functions.
2) **PWD mode**: set 1 to bit 11 of register 0 will put RTL8201 into power down mode. This is the maximum power saving mode when RTL8201 still alive. In PWD mode, RTL8201 will turn off all analog/digital function except MDC/MDIO manage interface. So if putting RTL8201 into PWD mode and MAC want to recall the PHY, it must create the MDC/MDIO timing by itself (software).
3) **LDPS mode**: set 1 to bit 12 of register 17 or pull LDPS pin high will put RTL8201 into LDPS (Link Down Power Saving) mode. In LDPS mode, RTL8201 will detect the link status to decide whether turn off the transmit function or not. If link off, it will not transmit FLP or 100Mbps IDLE/10Mbps NLP but some signals similar to NLP. Once the receiver had detected any leveled signal, it will stop the signal and transmit FLP or 100Mbps IDLE/10Mbps NLP again. This may save for about 60%~80% of power when link down.

6.7 Repeater Mode operation

Setting 1 to bit 15 of register 17 or pull the RPTR pin high will set RTL8201 into repeater mode. In repeater mode, the RTL8201 will assert CRS high only when receiving packet. In NIC mode (default, RPTR pin pull low or set 0 to bit 15 of register 17) will assert CRS high both transmitting and receiving packet. So if using RTL8201 in repeater, please set RTL8201 to Repeater mode, if using RTL8201 in NIC or switch application, please set to the default mode.

6.8 Power, Rest and Transmit bias

The RTL8201 can be reset by pull low RESTB pin for about 10ms, then pull high the pin or just set 1 to bit 15 of register 0, and then set to 0. Rest will clear the registers and re-initialize them, the media interface will first disconnect and restart auto-negotiation/parallel detection process.

Digital power and Analog power(including PLLVDD) should be different, the analog power need some bead (100Ohm@100Mhz) and capacitor to reduce the power noise and sufficient decouple is also necessary.

The analog and digital Ground plane should be as large and intact as possible, so if the ground plane is large enough, we can separate the analog ground and digital ground, this is a more ideal configuration. But if the total ground plane is not sufficiently large, partition on the ground plane is not a good idea. In this case, we can simply connect all the ground pins together to a larger and intact ground plane.

The RTSET pin must be pulled low by 2.0K ohm resister with 1% accuracy to establish a accuracy transmit bias, this will affect the signal quality of transmit waveform. Keep away from other clock traces or transmit/receive path to avoid signal interference.

6.9 Serial Network Interface:

RTL8201 also support traditional 7-wire serial interface to cooperate with some legacy MACs or embedded systems. To setup for this mode operation, pull MII/SNIB pin low and by doing so, RTL8201 will ignore the setup of ANE and SPEED pins. In this mode, RTL8201 will default work on 10Mbps and Half-duplex mode. But RTL8201 may also support full duplex mode operation if the DUPLEX pin been pull high.

This interface consists of 10Mbps transmit and receive clock generated by PHY, 10Mbps transmit and receive serial data, transmit enable, collision detect, and carry sense signals.

6.10 Flow control support:

RTL8201 supports flow control indication, MAC can program the MII register to indicate PHY that flow control is supported. When MAC support Flow Control mechanic, setting bit 10 of ANAR register by MDC/MDIO interface, then RTL8201 will add the ability to its N-Way ability. If the Link partner also support Flow Control, then RTL8201 can recognize by Link partner' s N-Way ability by examine the bit 10 of ANLPAR(register 5).

7. Register Definitions

Definitions and usage for each of the registers listed below are provided on this and the following pages:

7.1 Register 0 - Basic Mode Control Register

Address	Name	Description/Usage	Default/ Attribute
0:<15>	Reset	This bit sets the status and control registers of the PHY in a default state. This bit is self-clearing. 1 = software reset; 0 = normal operation.	0, RW
0:<14>	Loopback	This bit enables loopback of transmit data nibbles TXD<3:0> to the receive data path. 1 = enable loopback; 0 = normal operation.	0, RW
0:<13>	Spd_Set	This bit sets the network speed. 1 = 100Mbps; 0 = 10Mbps.	1, RW
0:<12>	Auto Negotiation Enable	This bit enables/disables the NWay auto-negotiation function. 1 = enable auto-negotiation; bits 0:<13> and 0:<8> will be ignored. 0 = disable auto-negotiation; bits 0:<13> and 0:<8> will determine the link speed and the data transfer mode, respectively.	1, RW
0:<11>	Power Down	This bit turns down the power of the PHY chip including internal crystal oscillator circuit. The MDC, MDIO is still alive for accessing with MAC. 1 = power down; 0 = normal operation.	0, RW
0:<10>	Reserved		
0:<9>	Restart Auto Negotiation	This bits allows the NWay auto-negotiation function to be reset. 1 = re-start auto-negotiation; 0 = normal operation.	0, RW
0:<8>	Duplex Mode	This bit sets the duplex mode. 1 = full duplex; 0 = normal operation.	1, RW
0:<7:0>	Reserved		

7.2 Register 1 - Basic Mode Status Register

Address	Name	Description/Usage	Default/ Attribute
1:<15>	100Base-T4	1 = enable 100Base-T4 support; 0 = suppress 100Base-T4 support.	0, RO
1:<14>	100Base_TX _ FD	1 = enable 100Base-TX full duplex support; 0 = suppress 100Base-TX full duplex support.	1, RO
1:<13>	100BASE_T X_HD	1 = enable 100Base-TX half duplex support; 0 = suppress 100Base-TX half duplex support.	1, RO
1:<12>	10Base_T_F D	1 = enable 10Base-T full duplex support; 0 = suppress 10Base-T full duplex support.	1, RO
1:<11>	10_Base_T_ HD	1 = enable 10Base-T half duplex support; 0 = suppress 10Base-T half duplex support.	1, RO
1:<10:6>	Reserved		
1:<5>	Auto Negotiation Complete	1 = auto-negotiation process completed; 0 = auto-negotiation process not completed.	0, RO
1:<4>	Remote Fault	1 = remote fault condition detected (cleared on read); 0 = no remote fault condition detected.	0, RO
1:<3>	Auto Negotiation	1 = Link had not been experienced fail state. 0 = Link had been experienced fail state	1, RO
1:<2>	Link Status	1 = valid link established; 0 = no valid link established.	0, RO
1:<1>	Jabber Detect	1 = jabber condition detected; 0 = no jabber condition detected.	0, RO
1:<0>	Extended Capability	1 = extended register capability; 0 = basic register capability only.	1, RO

7.3. Register 2 – PHY Identifier Register 1

Address	Name	Description/Usage	Default/ Attribute
2:<15;0>	PHYID1	PHY identifier ID for software recognize RTL8201	0000, RO

7.4. Register 3 – PHY Identifier Register 2

Address	Name	Description/Usage	Default/ Attribute
3:<15;0>	PHYID2	PHY identifier ID for software recognize RTL8201	8201, RO

7.5. Register 4 - Auto-negotiation Advertisement Register (ANAR)

Address	Name	Description/Usage	Default/ Attribute
4:<15>	NP	Next Page bit. 0 = transmitting the primary capability data page; 1 = transmitting the protocol specific data page.	0, RO
4:<14>	ACK	1 = acknowledge reception of link partner capability data word.	0, RO
4:<13>	RF	1 = advertise remote fault detection capability; 0 = do not advertise remote fault detection capability.	0, RW
4:<12:11>	Reserved		
4:<10>	Pause	1 = flow control is supported by local node 0 = flow control is NOT supported by local node	0, RW
4:<9>	T4	1 = 100Base-T4 is supported by local node; 0 = 100Base-T4 not supported by local node.	0, RO
4:<8>	TXFD	1 = 100Base-TX full duplex is supported by local node; 0 = 100Base-TX full duplex not supported by local node.	1, RW
4:<7>	TX	1 = 100Base-TX is supported by local node; 0 = 100Base-TX not supported by local node.	1, RW
4:<6>	10FD	1 = 10Base-T full duplex supported by local node; 0 = 10Base-T full duplex not supported by local node.	1, RW
4:<5>	10	1 = 10Base-T is supported by local node; 0 = 10Base-T not supported by local node.	1, RW
4:<4:0>	Selector	Binary encoded selector supported by this node. Currently only CSMA/ CD <00001> is specified. No other protocols are supported.	<00001>, RW

7.6 Register 5 - Auto-Negotiation Link Partner Ability Register (ANLPAR)

Address	Name	Description/Usage	Default/ Attribute
5:<15>	NP	Next Page bit. 0 = transmitting the primary capability data page; 1 = transmitting the protocol specific data page.	0, RO
5:<14>	ACK	1 = link partner acknowledges reception of local node' s capability data word.	0, RO
5:<13>	RF	1 = link partner is indicating a remote fault.	0, RO
5:<12:11>	Reserved		
5:<10>	Pause	1 = flow control is supported by Link partner 0 = flow control is NOT supported by Link partner	0, RO
5:<9>	T4	1 = 100Base-T4 is supported by link partner; 0 = 100Base-T4 not supported by link partner.	0, RO
5:<8>	TXFD	1 = 100Base-TX full duplex is supported by link partner; 0 = 100Base-TX full duplex not supported by link partner.	0, RO
5:<7>	TX	1 = 100Base-TX is supported by link partner; 0 = 100Base-TX not supported by link partner.	1, RO
5:<6>	10FD	1 = 10Base-T full duplex is supported by link partner; 0 = 10Base-T full duplex not supported by link partner.	0, RO
5:<5>	10	1 = 10Base-T is supported by link partner; 0 = 10Base-T not supported by link partner.	0, RO
5:<4:0>	Selector	Link Partner's binary encoded node selector. Currently only CSMA/ CD <00001> is specified.	<00000>, RO

7.7 Register 6 - Auto-negotiation Expansion Register (ANER)

Address	Name	Description/Usage	Default/ Attribute
6:<15:5>	Reserved	This bit is always set to 0.	
6:<4>	MLF	Status indicating if a multiple link fault has occurred. 1 = fault occurred; 0 = no fault occurred.	0, RO
6:<3>	LP_NP_ABLE	Status indicating if the link partner supports Next Page negotiation. 1 = supported; 0 = not supported.	0, RO
6:<2>	NP_ABLE	This bit indicates if the local node is able to send additional Next Pages.	0, RO
6:<1>	PAGE_RX	This bit is set when a new Link Code Word Page has been received. The bit is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.	0, RO
6:<0>	LP_NW_ABLE	1 = link partner supports NWay auto-negotiation.	0, RO

7.8 Register 16 Nway Setup Register (NSR)

Address	Name	Description/Usage	Default/ Attribute
16:<15:12>	Reserved		
16:<11>	ENNWLE	1 = LED4 Pin indicates linkpulse	RW
16:<10>	Testfun	1 = Auto-neg speeds up internal timer	0, RW
16:<9>	NWLPBK	1 = set NWay to loopback mode.	0, RW
16:<8;3>	Reserved		
16:<2>	FLAGABD	1 = Auto-neg experienced ability detect state	0, RO
16:<1>	FLAGPDF	1 = Auto-neg experienced parallel detection fault state	0, RO
16:<0>	FLAGLSC	1 = Auto-neg experienced link status check state	0, RO

7.9 Register 17 - Loopback, Bypass, Receiver Error Mask Register (LBREMR)

Address	Name	Description/Usage	Default/ Attribute
17:<15>	RPTR	Set 1 to put RTL8201 into repeater mode	0, RW
17:<14>	BP_4B5B	Assertion of this bit allows bypassing of the 4B/5B & 5B/4B encoder.	0, RW
17:<13>	BP_SCR	Assertion of this bit allows bypassing of the scrambler/descrambler.	0, RW
17:<12>	LDPS	Set 1 to enable Link Down Power Saving mode	0, RW
17:<11>	AnalogOFF	Set 1 to power down analog function of transmitter and receiver.	0, RW
17:<10>	Reserved		
17:<9:8>	LB<1:0>	LB<1:0> are register bits for loopback control as defined below: 1) 0 0 for normal mode; 2) 0 1 for PHY loopback; 3) 1 0 for twister loopback	<0, 0>, RW
17:<7>	F_Link_100	Used to logic force good link in 100Mbps for diagnostic purposes.	1, RW
17:<6:5>	Reserved		
17:<4>	CODE_err	Assertion of this bit causes code error detection to be reported.	0, RW
17:<3>	PME_err	Assertion of this bit causes pre-mature end error detection to be reported.	0, RW
17:<2>	LINK_err	Assertion of this bit causes link error detection to be reported.	0, RW
17:<1>	PKT_err	Assertion of this bit causes detection of packet errors due to 722 ms time-out to be reported.	0, RW
17:<0>	RWPara	Parameter access enable, set 1 to access register 20~24	0, RW

7.10 Register 18 - RX_ER Counter (REC)

Address	Name	Description/Usage	Default/ Attribute
18:<15:0>	RXERCNT	This 16-bit counter increments by 1 for each valid packet received.	h'[0000], RW

7.11 Register 19 - 10Mbps Network Interface Configuration Register

Address	Name	Description/Usage	Default/ Attribute
19:<15:6>	Reserved		
19:<5>	LD	Active low TPI link disable signal. When low TPIstilltransmit link pulses and TPI stays in good link state.	1, RW
19:<4:2>	Reserved		
19:<1>	HBEN	Hart beat enable	0, RO
19:<0>	JBEN	1 = enable jabber function. 0 = disable jabber function	1, RW

7.12 Register 20 – PHY 1_1 Register

Address	Name	Description/Usage	Default/ Attribute
20:<15:0>	PHY1_1	PHY 1 register (functions as RTL8139C<78>)	R/W

7.13 Register 21 – PHY 1_2 Register

Address	Name	Description/Usage	Default/ Attribute
21:<15:0>	PHY1_2	PHY 1 register (functions as RTL8139C<78>)	R/W

7.13 Register 22 – PHY 2 Register

Address	Name	Description/Usage	Default/ Attribute
22<15:8>	PHY2_76	PHY2 register for cable length test (functions as RTL8139C<76>)	RO
22:<7:0>	PHY2_80	PHY2 register for PLL select (functions as RTL8139C<80>)	R/W

7.14 Register 23 – Twister_1 Register

Address	Name	Description/Usage	Default/ Attribute
23:<15:0>	TW_1	Twister register (functions as RTL8139C<7c>)	R/W

7.15 Register 24 – Twister_2 Register

Address	Name	Description/Usage	Default/ Attribute
24:<15:0>	TW_2	Twister register (functions as RTL8139C<7c>)	R/W

8. Electrical Characteristics

8.1 D.C. Electric Characteristics

8.1.1. Absolute Maximum Ratings

Symbol	Conditions	Min.	Type.	Max.
Supply Voltage		3.0V	3.3V	3.6V
Storage Temp.		-55°C		125°C

8.1.2. Operating Conditions

Symbol	Conditions	Min.	Type.	Max.
Vcc	Supply voltage	3.0V	3.3V	3.6V
TA	Operating Temperature	0°C		70°C

8.1.3. Power Dissipation

Pldps: mW

Piso:

Panaoff:

Ppwd:

Pm100:

Pm10h

Pm10f:

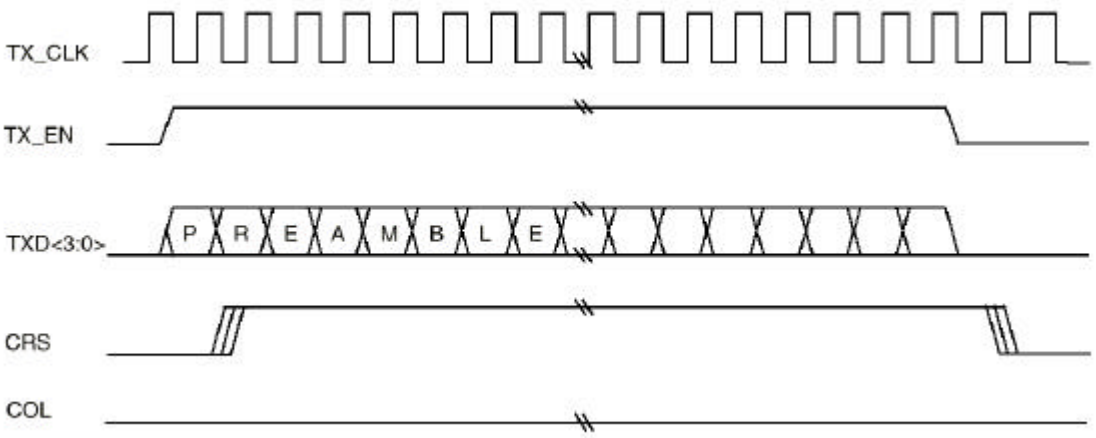
- Supply Voltage: Vcc

Symbol	Conditions		Min.	Type.	Max.
VIH	Input High Vol		0.5*Vcc		Vcc+0.5V
VIL	Input Low Vol.		-0.5V		0.3*Vcc
VOH	Output High Vol.	IOH=-8mA	0.9*Vcc		Vcc
VOL	Output Low Vol.	IOL=8mA			0.1*Vcc
IOZ	Tri-state Leakage	Vout=Vcc or GND	-10uA		10uA
Iin	Input Current	Vin=Vcc or GND	-1.0uA		1.0uA
Icc	Average Operating Supply Current	Iout=0mA		200mA	

8.2 A.C. Electric Characteristics

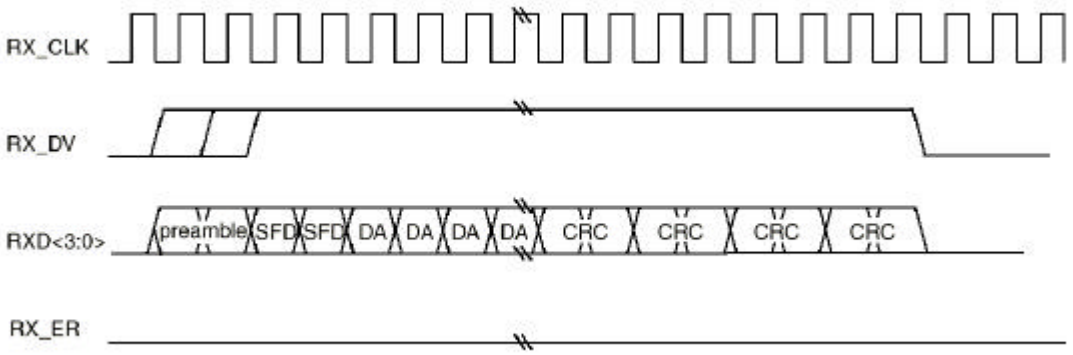
8.2.1 Transmission Without Collision

Shown is an example transfer of a packet from MAC to PHY.



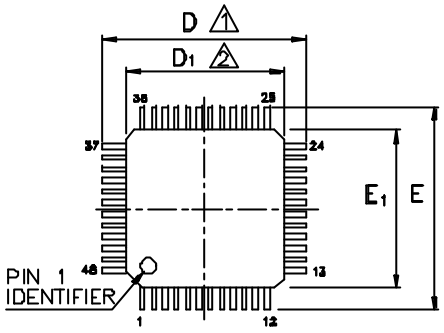
8.2.1 Reception Without Error

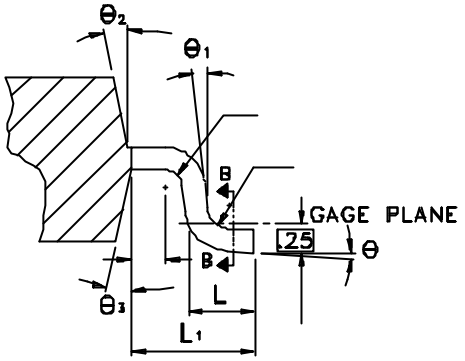
Shown is an example of transfer of a packet from PHY to MAC



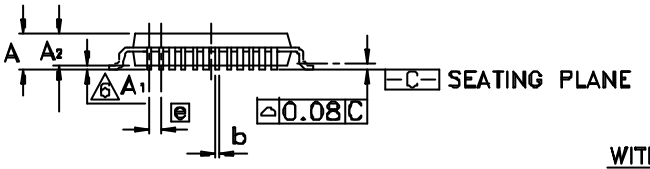
9. Application Circuit

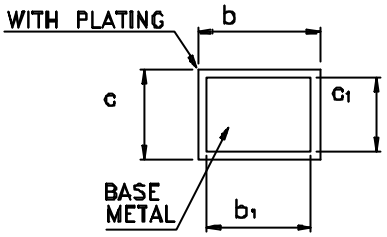
See Attachment





SECTION A–A





SECTION B–B

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	**0.1**	0.20
A2	0.051	0.055	0.059	1.30	**1.40**	1.50
b	0.006	0.009	0.011	0.15	**0.22**	0.29
b1	0.006	0.008	0.010	0.15	**0.20**	0.25
c	0.004	-	0.008	0.09	-	0.20
c1	0.004	-	0.006	0.09	-	0.16
D	0.354 BSC			9.00 BSC		
D1	0.276 BSC			7.00 BSC		
E	0.354 BSC			9.00 BSC		
E1	0.276 BSC			7.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L1	0.039 REF			1.00 REF		
q	0°	3.5°	9°	0°	3.5°	9°
q1	0°	-	-	0°	-	-
q2	12°TYP			12°TYP		
q3	12°TYP			12°TYP		

Note:

1.To be determined at seating plane -c-
2.Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3.Dimension b does not include dambar protrusion. Dambar can not be located on the lower radius of the foot.
4.Exact shape of each corner is optional.
5.These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7.Controlling dimension : millimeter.
8. Reference document : JEDEC MS-026 , BBC

TITLE : 48LD LQFP (7x7x1.4mm) PACKAGE OUTLINE DRAWING , FOOTPRINT 2.0mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	SS048 - P1
		DATE	Sept. 25.2000
REALTEK SEMI-CONDUCTOR CORP.			