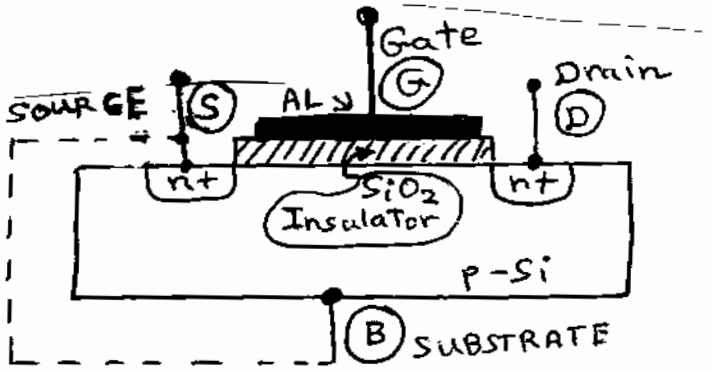
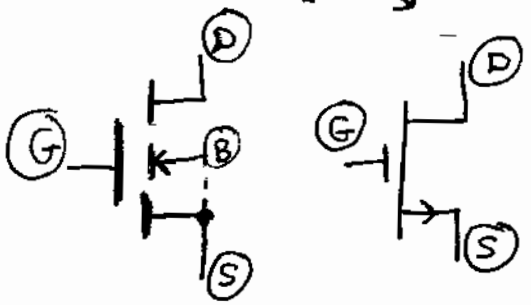
(Text 5.1) NMOSFET Model

MOSFET (1)

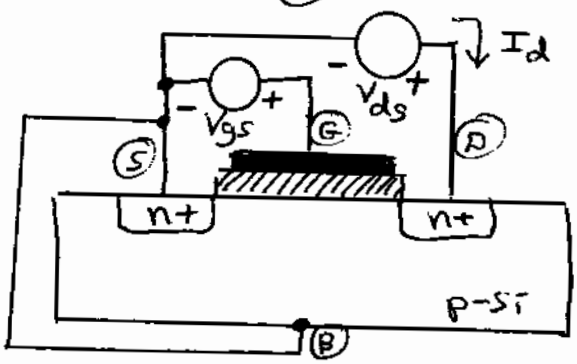
1. N-Channel Metal-Oxide Semiconductor Field Effect Transistor



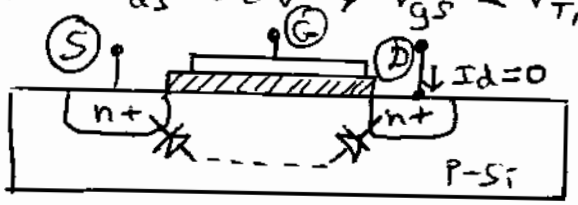
NMOSFET Symbols



Note that the NMOSFET is symmetrical, thus (S) and (D) are interchangeable. (D) is defined as the pin that is more positive than (S). Also, substrate (B) is usually connected to the source (S)



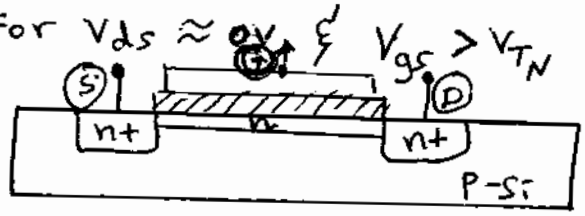
For $V_{ds} \approx 0V$ & $V_{gs} < V_{TN}$



⇒ Back-to-Back diodes in series
⇒ Cutoff NMOSFET
⇒ $I_d = 0$

V_{TN} ≙ "Threshold Voltage" (1V, 3V)

For $V_{ds} \approx 0V$ & $V_{gs} > V_{TN}$



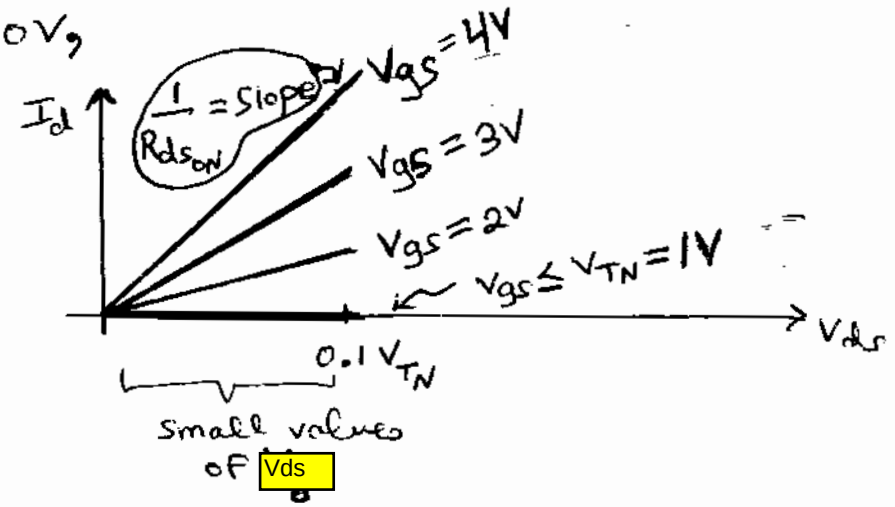
Thin n-type Conducting "inversion channel" opens up between (S) and (D) diffusions.
⇒ NMOSFET is ON!

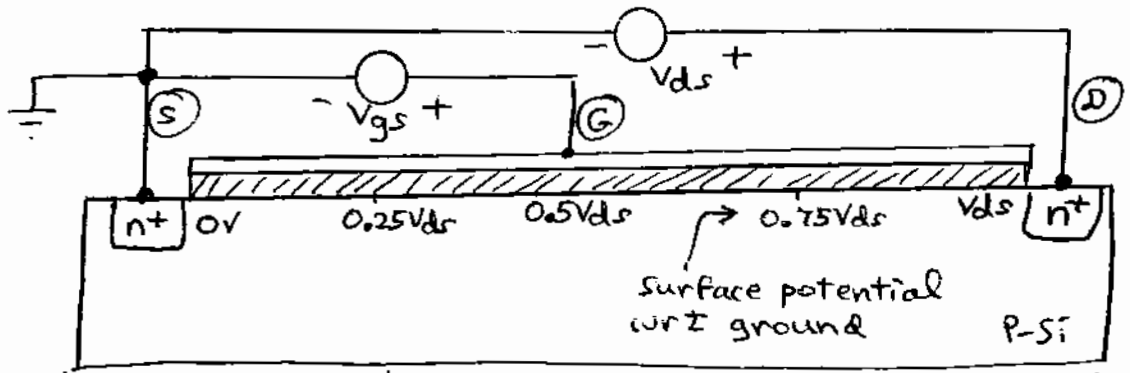
Two regions of operation for MOSFET w/ $V_{gs} > V_{T_N}$

A. Ohmic Region

For $V_{ds} \approx 0V$,

MOSFET acts like a (linear) Resistance $R_{ds_{ON}}$ that is controlled by V_{gs}





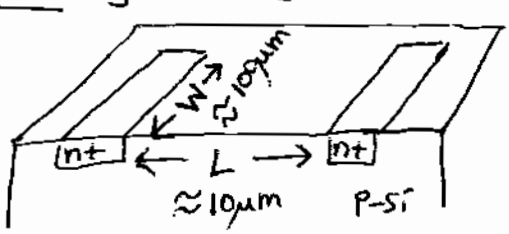
For nonzero V_{ds}, the surface potential just under the gate oxide distributes itself linearly, as shown above. For the conducting channel to extend all the way to the drain end, the G-to-surface potential, $V_{gs} - V_{ds} \geq V_{T_N}$. Under this condition, the NMOSFET operates in its "ohmic mode", where the I_d vs. V_{ds} curve is approximately linear for small V_{ds}, as shown above. It can be shown:

$$I_d = K_N \left[2 (V_{gs} - V_{T_N}) \cdot V_{ds} - V_{ds}^2 \right] \quad \left(\text{for } V_{gs} - V_{ds} > V_{T_N} \right)$$

where K_N is the "Conduction Parameter" given by

$$K_N \triangleq \frac{\mu_n \epsilon_0 \epsilon_{ox}}{2\, t_{ox}} \left(\frac{W}{L} \right)$$

- μ_n: surface mobility $\approx 600 \frac{cm^2}{V \cdot s}$
- ϵ_0: 8.85×10^{-14} F/cm
- ϵ_{ox}: 3.9
- t_{ox}: SiO_2 oxide thickness $\approx 0.1\mu m$
- W: channel width
- L: channel length



Typ. Value $K_N = 100\mu A/V^2$

B. Saturation Region

For $\boxed{V_{gs} - V_{ds} < V_{T_N}}$

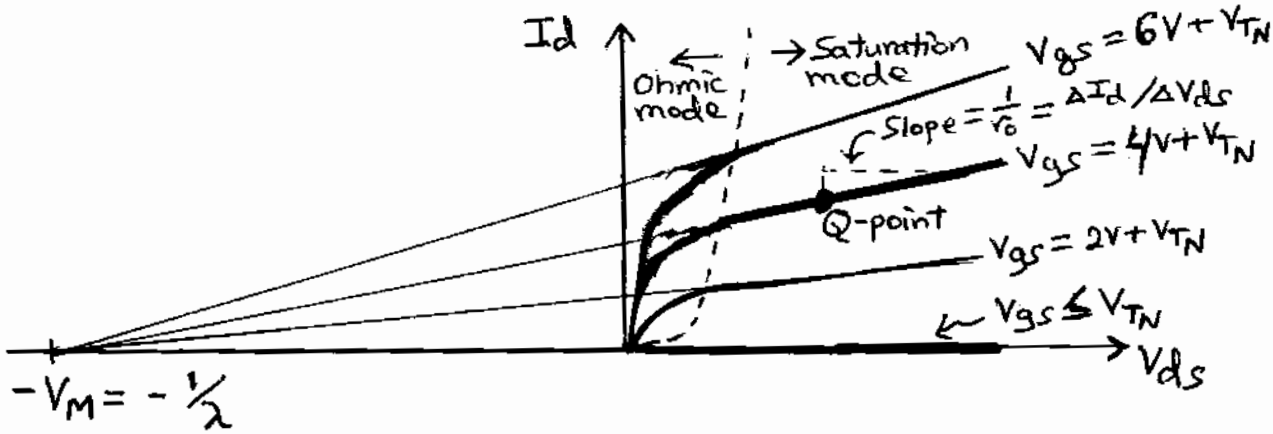
The conducting channel ends (is "pinched off") somewhere to the left of the drain diffusion, and the drain current no longer rises as V_{ds} is increased above the point where $V_{gs} - V_{ds} = V_{T_N} \Rightarrow V_{ds} = V_{gs} - V_{T_N}$.

Therefore I_{ds} can be found by replacing V_{ds} by $V_{gs} - V_{T_N}$ in the ohmic region equation

$$I_d = K_n \left[2(V_{gs} - V_{T_N}) \underbrace{(V_{gs} - V_{T_N})}_{V_{ds}} - \underbrace{(V_{gs} - V_{T_N})^2}_{V_{ds}} \right]$$

$$I_d = K_n \left[V_{gs} - V_{T_N} \right]^2$$

A secondary (not so important) effect of "channel length modulation" occurs as V_{ds} in increased well beyond $V_{gs} - V_{T_N}$ and the pinchoff point moves away from the drain toward the source. The channel length is shortened, making the current rise slightly, causing the "horizontal" part of the I_d vs. V_{ds} curve to slope slightly upward.



To account for this slight upward slope we define the "channel length modulation constant", λ

For $V_{gs} - V_{ds} < V_{TN}$

$$I_d = K_N (V_{gs} - V_{TN})^2 (1 + \lambda \cdot V_{ds})$$

↑ Typical values of λ $(0.005 < \lambda < 0.03)\ V^{-1}$

Note that this family of curves (each curve corresponds to a different V_{gs} value) must all pass through $I_d = 0$ at the value of V_{ds} where

$$(1 + \lambda \cdot V_{ds}) = 0$$

$$\Rightarrow V_{ds} = -\frac{1}{\lambda} = -V_M$$

$V_M = 1/\lambda$ is analogous to the "Early Voltage" in a BJT.

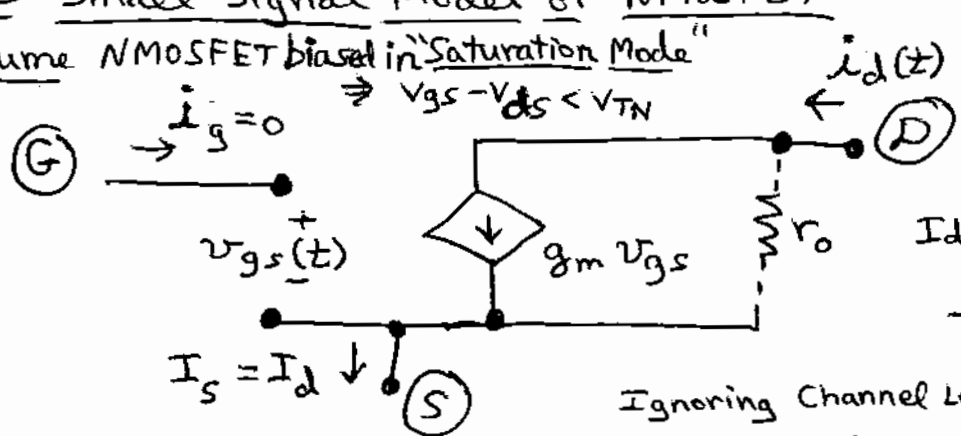
Typically $200V > V_M > 33.3V$

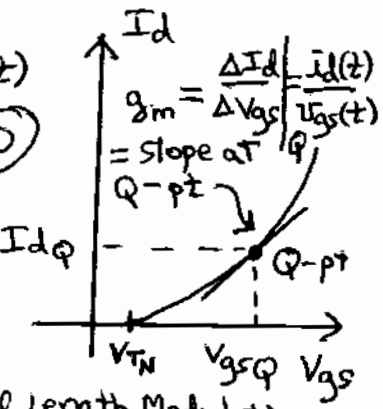
Often λ is assumed to be zero ($V_M = \frac{1}{0} = \infty$) in a hand calculation.

C. Cutoff Region $V_{gs} < V_{TN}$ NMOSFET is OFF, as mentioned on page (1), and $\boxed{I_d = 0}$

2. AC Small-Signal Model of NMOSFET

Assume NMOSFET biased in "Saturation Mode" $\Rightarrow V_{gs} - V_{ds} < V_{TN}$





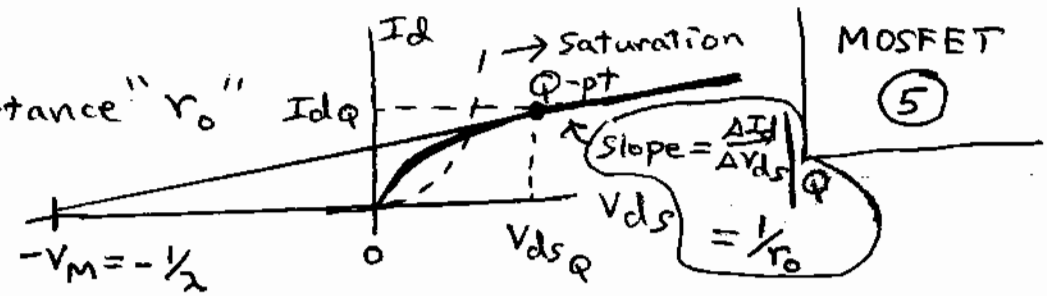
Ignoring Channel Length Modulation

$$I_d = K_N (V_{gs} - V_{TN})^2$$

$$= K_N \left[V_{gs}^2 - 2 V_{gs} V_{TN} + V_{TN}^2 \right]$$

$$\therefore g_m = \left. \frac{dI_d}{dV_{gs}} \right|_Q = \left. 2K_N \left[V_{gs} - V_{TN} \right] \right|_Q = \boxed{2K_N \left[V_{gs_Q} - V_{TN} \right]}$$

Output Resistance "r_o"



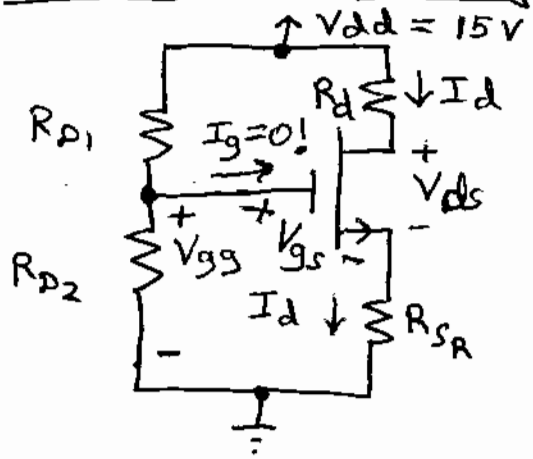
$$\frac{1}{r_o} = \frac{I_{dQ}}{V_M + V_{dsQ}} \cong \frac{I_{dQ}}{V_M} = \boxed{\lambda I_{dQ}}$$

($V_M + V_{dsQ}$: several hundred volts; V_M: several volts)

$$\boxed{r_o = \frac{1}{\lambda I_{dQ}}}$$

$$\boxed{g_m = 2K_N [V_{gsQ} - V_{T_N}]}$$

3. NMOSFET DC Biasing Example



Given an NMOSFET with

$K_N = 0.25 \frac{mA}{V^2}$ and $V_{T_N} = 2V$

We wish to bias the MOSFET with

$I_{dQ} = 1mA$ and $V_{DD} = 15V$

such that we have equal voltage drops $\frac{Vdd}{3} = 5V$ across R_d, V_{ds}, and R_{S_R}.

Solution: Find required V_{gs}. Assume $V_{ds} = 5V$ (as desired)

Assume $(V_{gs} - 5V) < 2V$ (V_{ds}, V_{T_N}) $\Rightarrow$ Saturation Mode, otherwise NMOSFET will not amplify properly. We'll check this after V_{gs} is calculated.

$$I_D = K_N (V_{gs} - V_{T_N})^2 \Rightarrow V_{gs} = \begin{cases} 4V. \\ \cancel{0V.} \rightarrow \text{Reject 2nd solution, since } V_{gs} \text{ must be} > V_{T_N}! \end{cases}$$

(I_D: 1mA, K_N: 0.25 mA/V, V_{T_N}: 2V)

∴ NMOSFET Is saturated since

$$V_{gs} - V_{ds} = 4 - 5 = -1V < V_{T_N}$$

(V_{gs}: 4V, V_{ds}: 5V, V_{T_N}: 2V)

We require a 5V drop across $R_{S_R} \Rightarrow V_{gg} = V_{gs} + 5V = 9V$ (4V)

Thus we may choose R_{D_2} to be any convenient value (preferrably large), and then find R_{D_1} from the voltage divider formula.

$$\boxed{\text{Let } R_{D_2} = 1M\Omega}$$

(R_{D_2}: 1MΩ)

$$V_{dd} \cdot \frac{R_{D_2}}{R_{D_1} + R_{D_2}} = 9V \Rightarrow \boxed{R_{D_1} = 666.7\,k\Omega}$$

(V_{dd}: 15V, R_{D_2}: 1MΩ)

$$R_{S_R} = \frac{5V}{I_D} = \frac{5V}{1mA} = \boxed{5k\Omega}$$

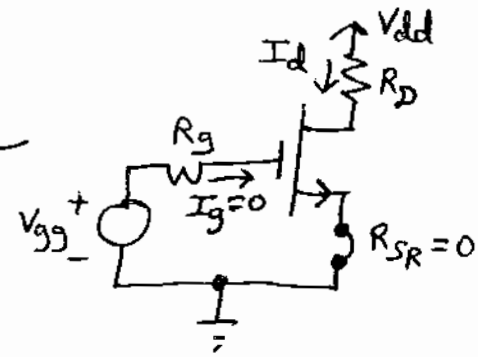
$$R_D = \frac{5V}{I_D} = \frac{5V}{1mA} = \boxed{5k\Omega}$$

Role of R_{S_R} in stabilizing Q-point w.r.t. changes in K_N and V_{T_N}:

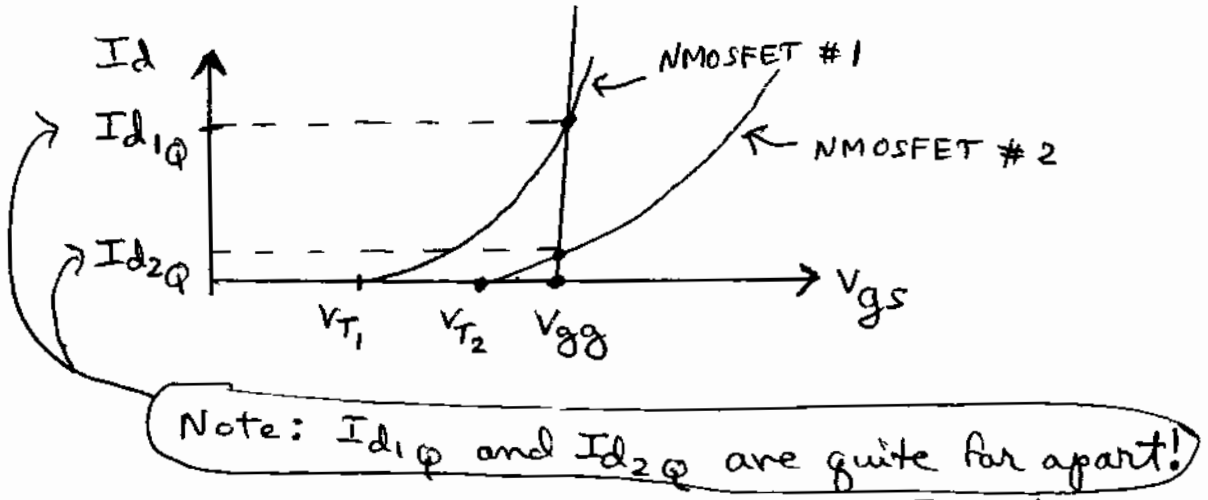
IF R_{S_R} is not used ($R_{S_R} = 0$), then

$$V_{gs} = V_{gg} = V_{DD} \frac{R_{D2}}{R_{D_2} + R_{D_1}}$$

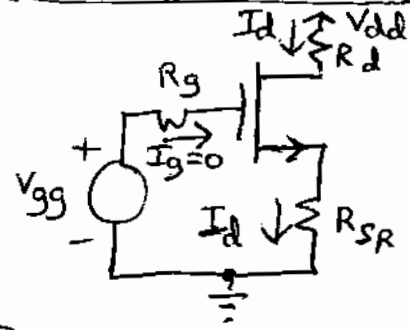
(Since $I_g = 0$)



Then for two widely different NMOSFET's (different K_N and V_{T_N} values), the vertical load line intersects at widely different I_D values, yielding a LARGE variation in dc bias Q-point!



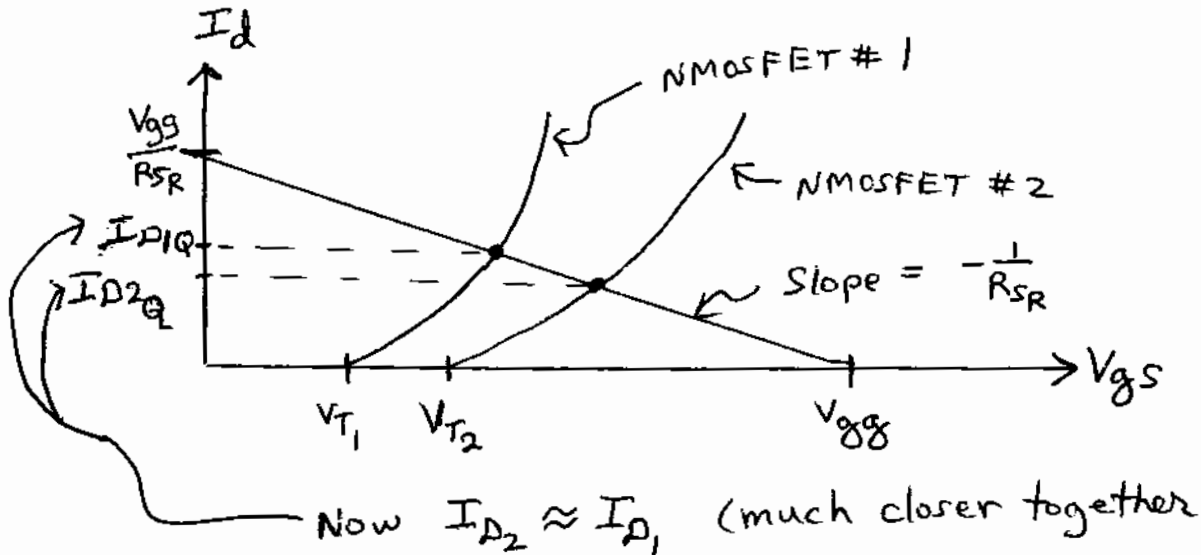
Now if R_{S_R} is present



$$V_{gg} = V_{gs} + I_d R_{S_R}$$

Solving for I_d

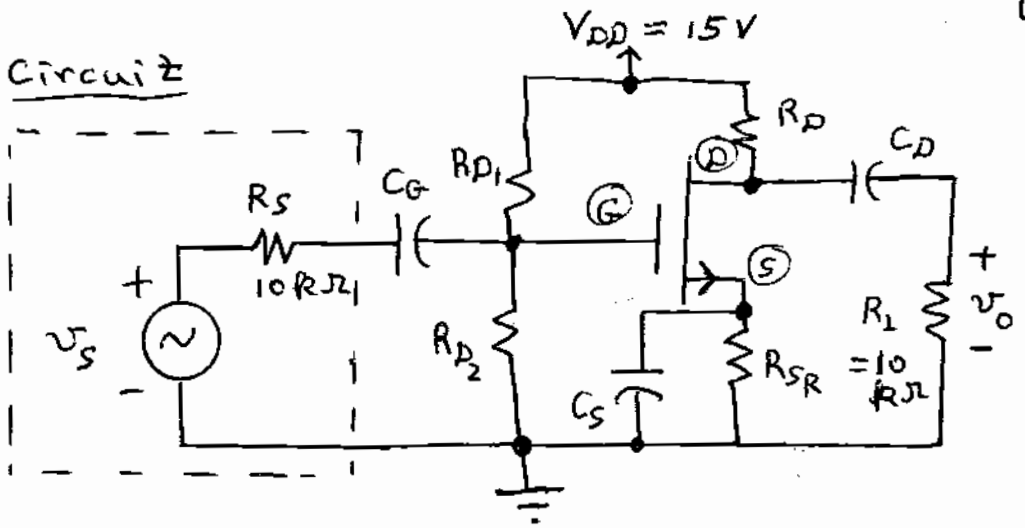
$$I_d = \frac{-1}{R_{S_R}} \cdot V_{gs} + \frac{V_{gg}}{R_{S_R}} \Rightarrow \begin{cases} I_d \text{ intercept} = V_{gg}/R_{S_R} \\ V_{gs} \text{ intercept} = V_{gg} \end{cases}$$



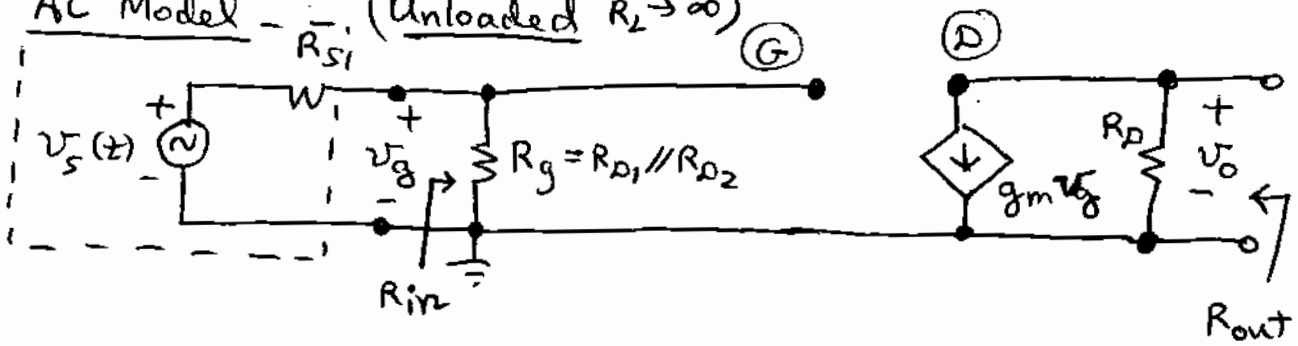
Note that the larger R_{S_R} is made, the better the bias stabilization... but the dc bias Q-point will be adversely affected if R_S is TOO LARGE!

4. NMOSFET Common-Source Amplifier

Circuit



AC Model – (Unloaded $R_L \to \infty$)



$$A_{V_o} = \frac{v_o}{v_g} = \frac{-R_D \cdot g_m v_g}{v_g} = \boxed{-g_m R_D}$$

$$R_{in} = R_g$$

$$R_{out} = R_D$$

For the choice of bias point chosen above ($I_{DQ} = 1mA, V_{DSQ} = 5V$)

$R_{D_1} = 666.7\ k\Omega$ $R_{D_2} = 1M\Omega$ $R_{S_R} = 5k\Omega$ $R_D = 5k\Omega$

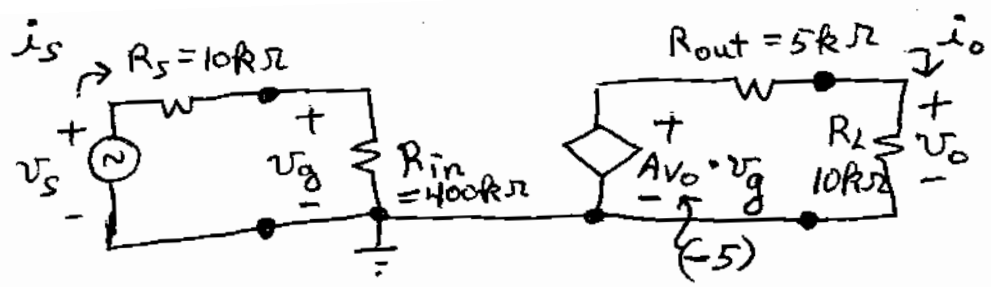
$V_{GS_Q} = 4V$ NMOSFET Parameters: $K_N = 0.25 \frac{mA}{V^2}$, $V_{T_N} = 2V$

$$\Rightarrow g_m = 2K_N(V_{GS_Q} - V_{T_N}) = 2\left(0.25 \frac{mA}{V^2}\right)(4-2) = 1 \frac{mA}{V}$$

$$A_{V_o} = -g_m R_D = -\left(1 \frac{mA}{V}\right)(5k\Omega) = \boxed{-5}$$

$R_{out} = R_D = 5k\Omega$

$R_{in} = R_G = R_{D_1} /\!/ R_{D_2} = 400k\Omega$



$$A_v = \left(\frac{400}{400+10}\right)\cdot(-5)\cdot\left(\frac{10}{10+5}\right) = \boxed{-3.25}$$

$$A_i = \frac{i_o}{i_s} = \frac{v_o/R_L}{v_s/(R_s+R_{in})} = A_v\cdot\left(\frac{R_s+R_{in}}{R_L}\right) = (-3.25)\left(\frac{410k}{10k}\right) = \boxed{-133.25}$$

$$A_p = \frac{i_o v_o}{i_s v_s} = A_i \cdot A_v = (-3.25)(-133.25) = \boxed{433}$$

Note that the voltage gain of MOSFET amplifier is lower than a BJT amplifier ... BUT its input impedance is higher ⇒ higher current gain, resulting in an "A_p" that is comparable to a BJT amplifier!

5. PSPICE Simulation of MOSFET Amplifier

To simulate in PSPICE you need to know that the PSPICE MOSFET models define the conduction parameter as "KP" (process gain), where

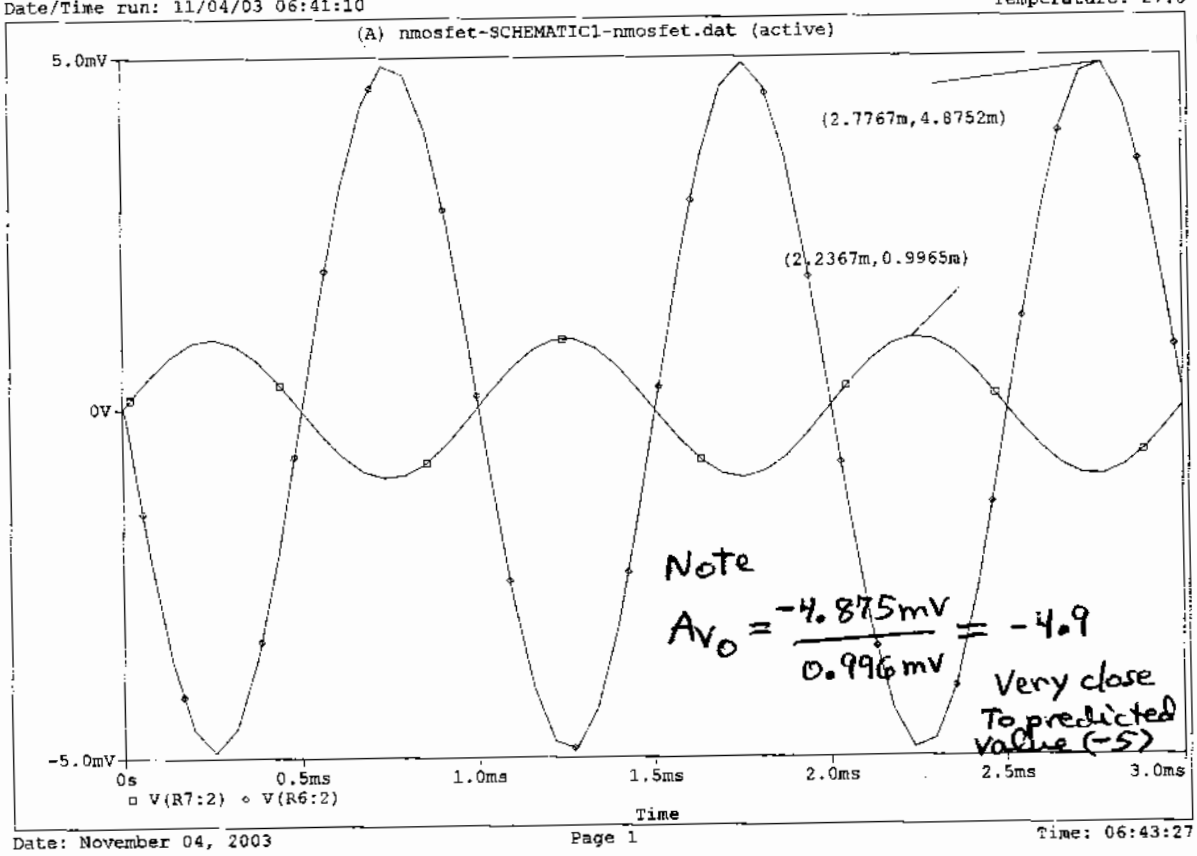
$$K_N \triangleq \frac{W}{2L} KP \Rightarrow KP = \frac{2L}{W} K_N$$

Thus, to specify K_N in PSPICE, you must set three parameters: KP, W, and L.

- KP ↑ process gain
- W ↑ channel width
- L ↑ channel length

For example, to simulate the above circuit, choose the IRF150, (EVAL Library), and make W = 2u, L = 1u, KP = 250u, VTO = 2.0V (PSPICE calls V_{TN} "VTO")

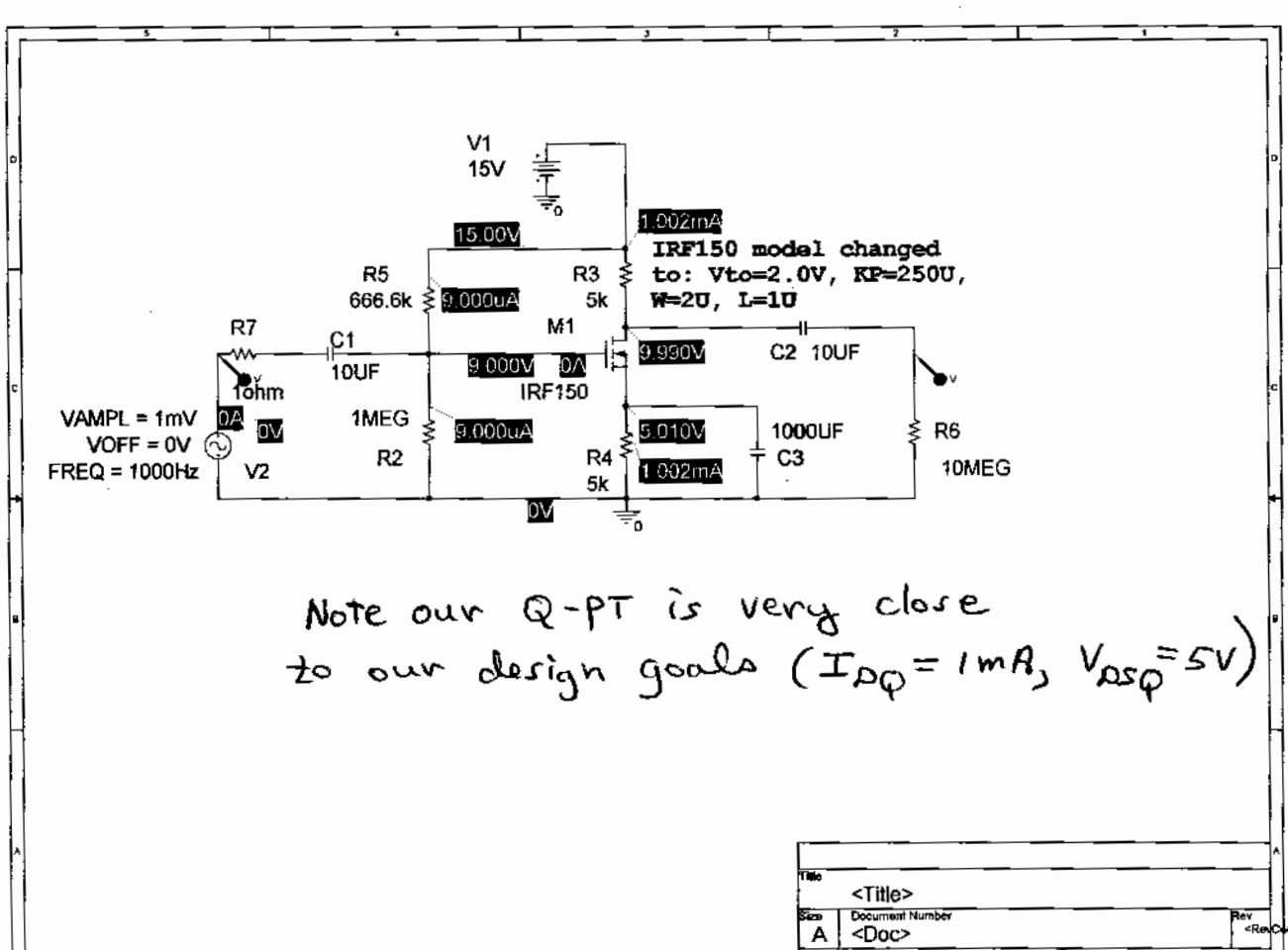
MOSFET
(19)



Note

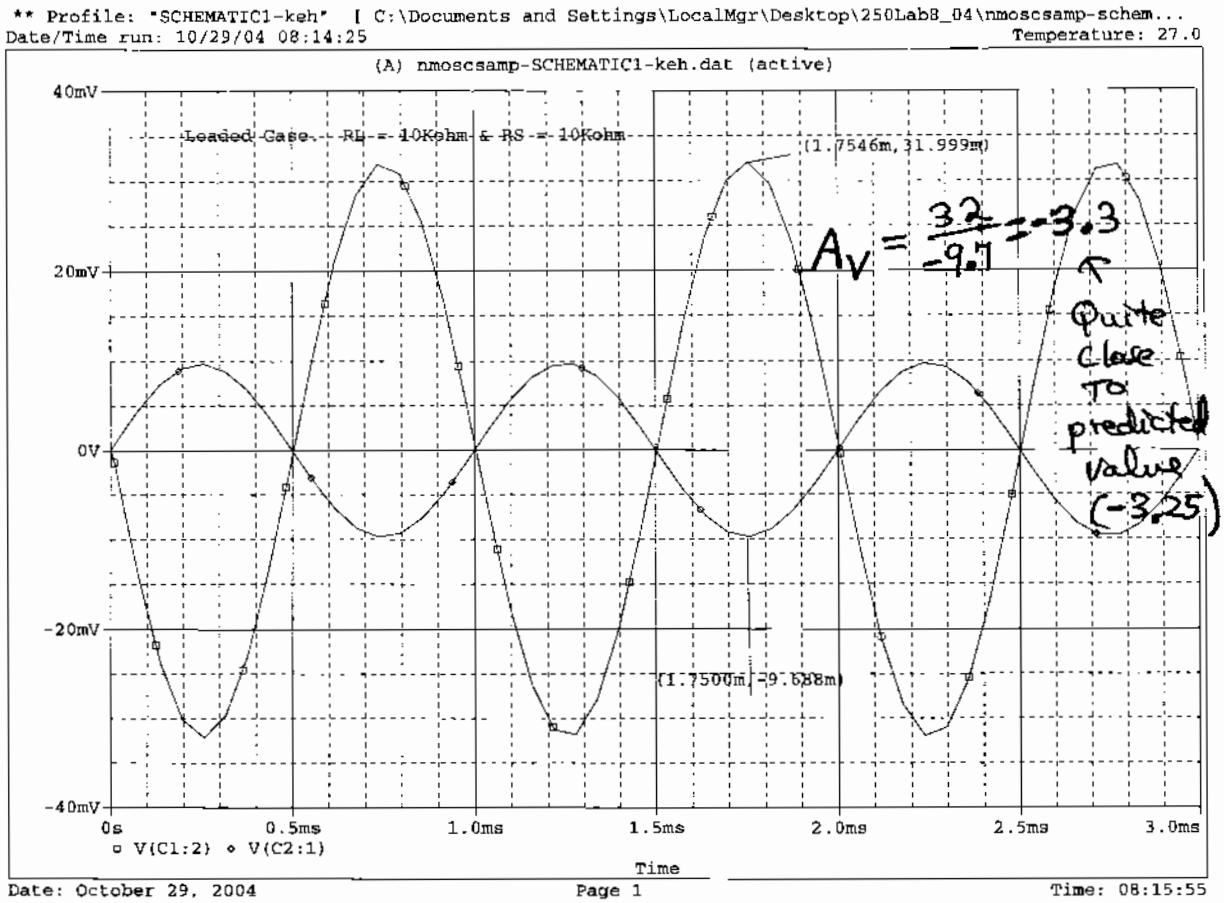
$$Av_o = \frac{-4.875mV}{0.996mV} = -4.9$$

Very close To predicted value (-5)



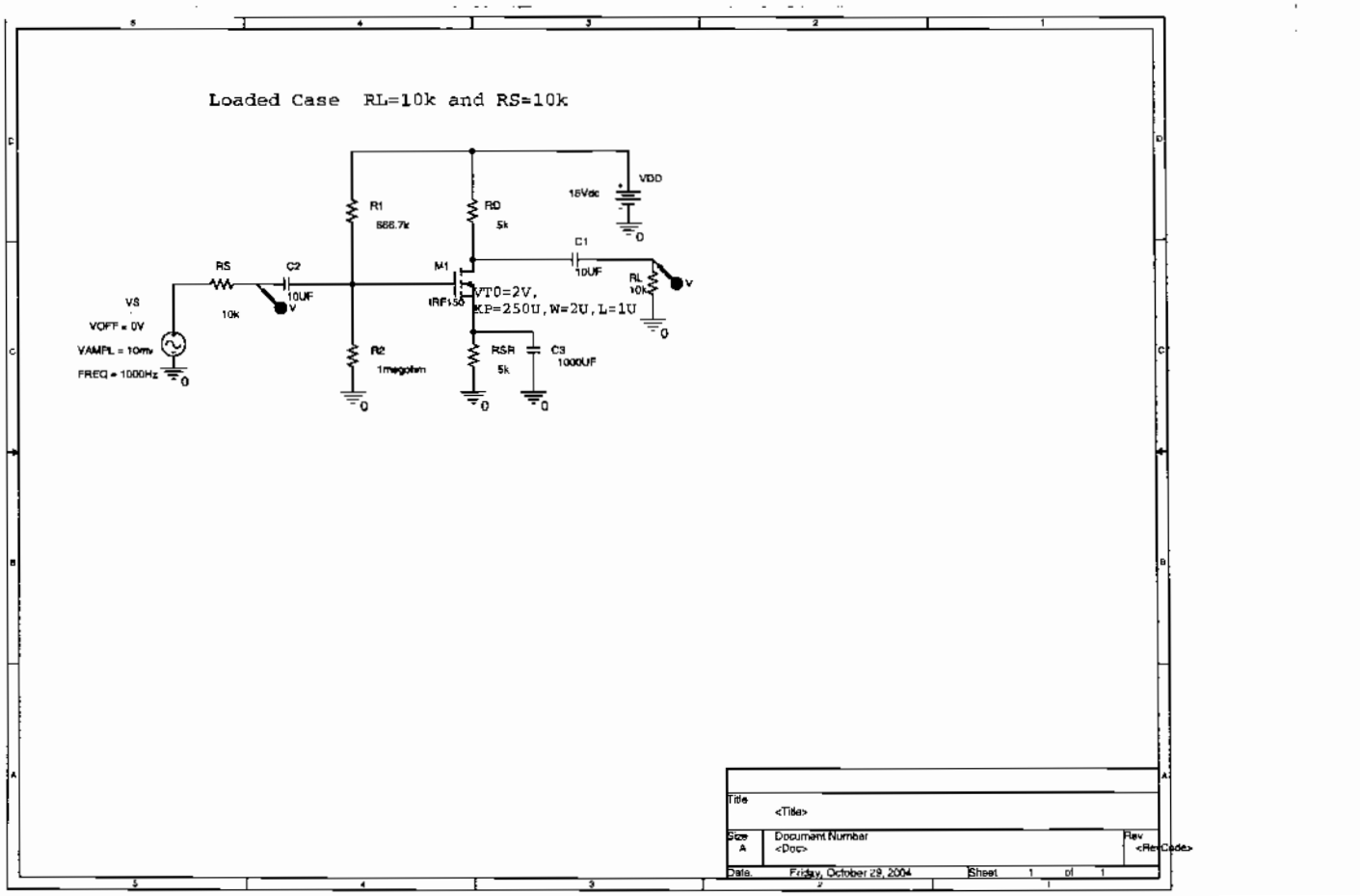
Note our Q-PT is very close to our design goals ($I_{DQ} = 1mA$, $V_{DSQ} = 5V$)

MOSFET 10B

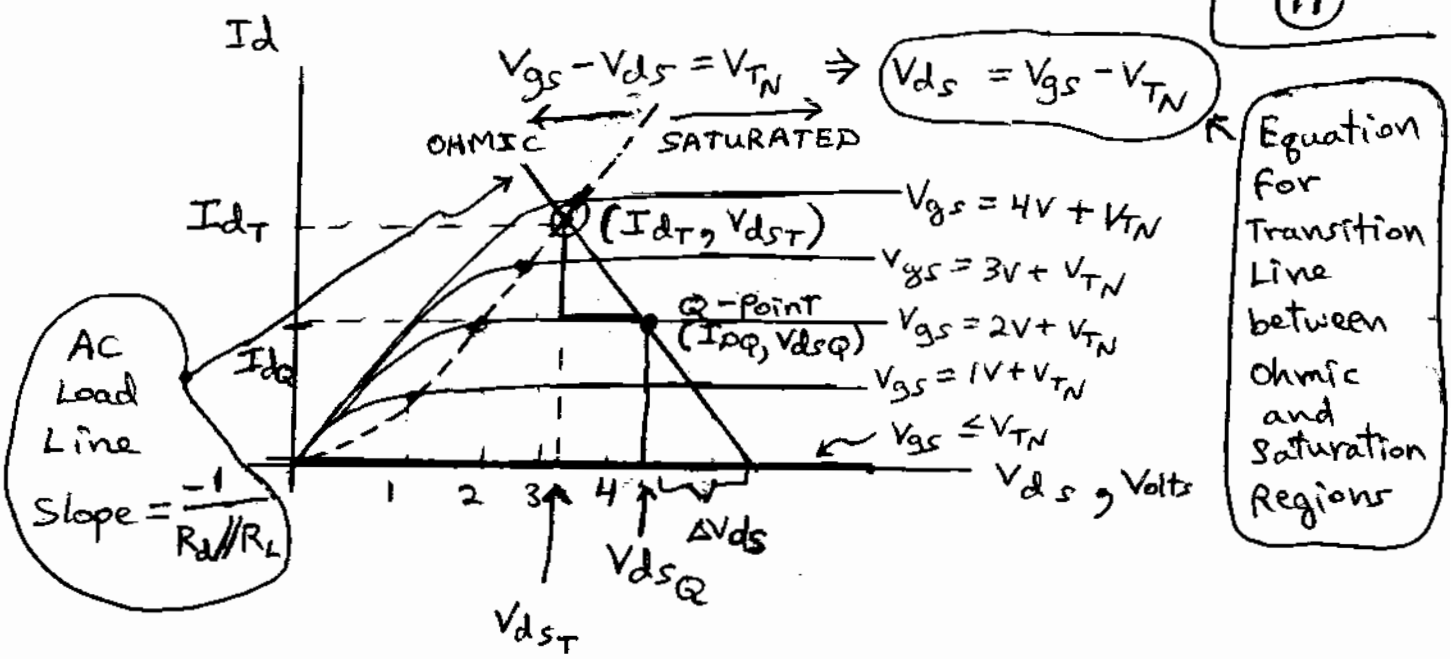


$A_V = \frac{32}{-9.7} = -3.3$

↑ Quite close to predicted value (-3.25)



6. Maximum Symmetrical V_{ds} Output Swing



Finding "Transition Point" (I_{d_T}, V_{ds_T}) on AC loadline, where MOSFET leaves saturation mode (the amplifying region) and enters ohmic mode.

$$\text{SLOPE AC Loadline} = \frac{-1}{R_d // R_L} = \frac{I_{dQ} - I_{d_T}}{V_{dsQ} - V_{ds_T}}$$

But (in saturation) $I_{d_T} = K_N (V_{gs_T} - V_{T_N})^2$

$$\Rightarrow V_{gs_T} = \pm\sqrt{\frac{I_{d_T}}{K_N}} + V_{T_N} = \sqrt{\frac{I_{d_T}}{K_N}} + V_{T_N}$$

(Reject solution for $V_{gs_T} < V_{T_N}$)

From equation for transition line between ohmic and saturation regions:

$$V_{ds_T} = V_{gs_T} - V_{T_N}$$

$$V_{ds_T} = \sqrt{\frac{I_{d_T}}{K_N}} + \cancel{V_{T_N}} - \cancel{V_{T_N}} \Rightarrow I_{d_T} = K_N V_{ds_T}^2$$

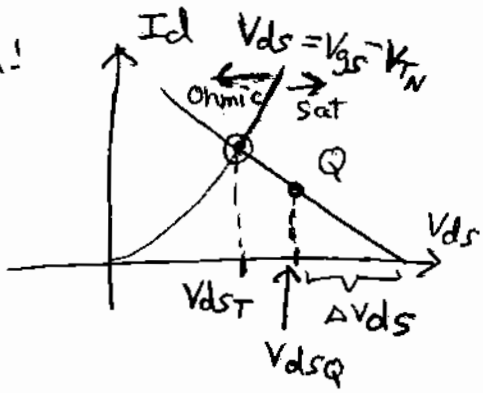
$$\therefore \text{Slope of AC Loadline} = \frac{-1}{R_d // R_L} = \frac{I_{dQ} - K_N V_{ds_T}^2}{V_{dsQ} - V_{ds_T}}$$

In our example,

$$\frac{-1}{5R\,//\,10R} = \frac{1mA - 0.25\frac{mA}{V^2}(V_{ds_T}^2)}{(5V - V_{ds_T})}$$

$$\Rightarrow V_{ds_T} = -3.818V \text{ (omit negative solution!)},\ \boxed{2.619V}$$

$$I_{d_T} = K_N V_{ds_T}^2 = \boxed{1.71mA}$$



$$\frac{-1}{R_D\,//\,R_L} = \frac{-I_{dQ}}{\Delta V_{ds}}$$

$$\frac{-1}{5R\,//\,10R} = \frac{-1mA}{\Delta V_{ds}} \Rightarrow \Delta V_{ds} = 3.33V$$

Compare:

$V_{dsQ} - V_{ds_T} = 5V - 2.619V = 2.38V$ ← smaller value

∴ Max symmetrical V_{ds} Swing $= 2(2.38) = \boxed{4.76\ V.\ \text{peak-peak}}$

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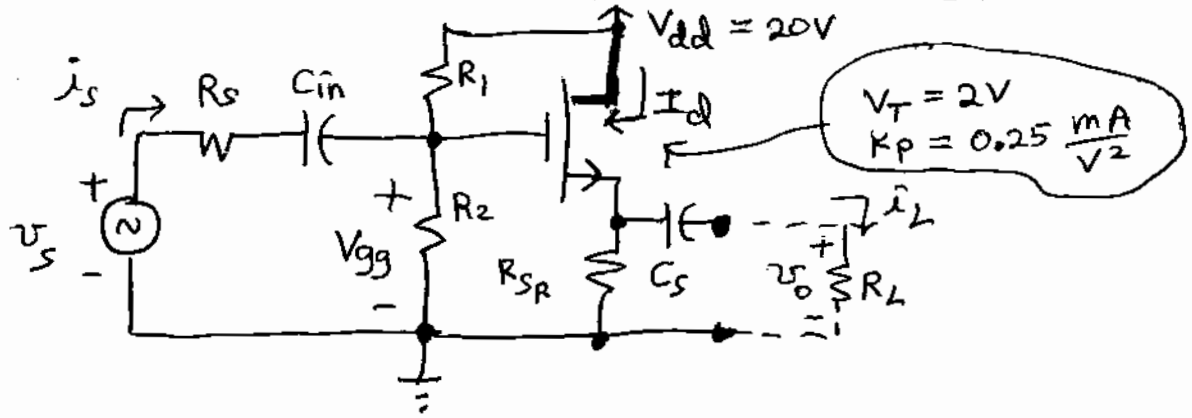
7. NMOSFET COMMON-DRAIN (SOURCE-FOLLOWER) Amplifier



Let us choose to bias the NMOSFET at $V_{ds} = V_{dd}/2 = 10V$

Also let us choose a bias drain current

$$I_{dQ} = 5mA$$

MOSFET (13)

Assume $V_{dd} = 20V$, $V_{T_N} = 2V$, $K_N = 0.25 \frac{mA}{V^2}$, $\lambda = 0.01$ 1/V $\Rightarrow V_M = 100V$

Solution

Assume NMOSFET is saturated (we can check this later.)

$$I_{dQ} = K_N (V_{gsQ} - V_{T_N})^2 \Rightarrow$$

(I_{dQ}: 5mA; K_N: 0.25×10^{-3} A/V^2; V_{T_N}: 2V)

$V_{gsQ} = -2.47$ (reject, $< V_{T_N}$), $6.472V$

Note $V_{dsQ} = 20 - 10 = 10V$

$\therefore V_{gsQ} - V_{dsQ} = 6.47 - 10 < 2V$ (V_{T_N})

$\Rightarrow$ Saturated!

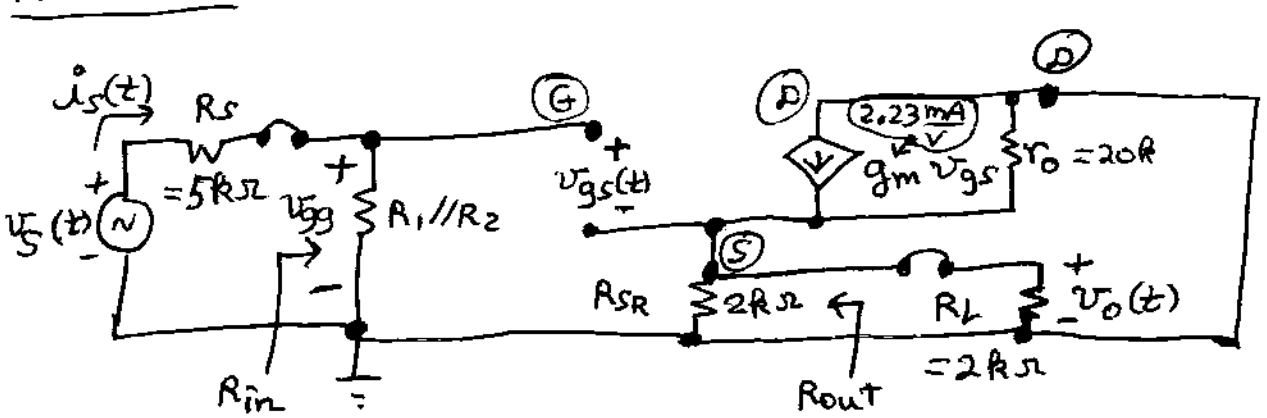
KVL: $V_{gg} = V_{gs} + \underbrace{\frac{V_{dd}}{2}}_{\text{(desired } V_{R_{SR}})}$ $\Rightarrow V_{gg} = 6.472V + \frac{20V}{2} = 16.472V$

$$R_{SR} = \frac{V_{dd}/2}{I_d} = \frac{(20V/2)}{5mA} = \boxed{2k\Omega}$$

Arbitrarily choosing $\boxed{R_1 = 1M\Omega}$ (some high value)

$$V_{gg} = 16.472V = 20V \left(\frac{R_2}{R_1 + R_2} \right) \Rightarrow \boxed{R_2 = 4.67M\Omega}$$

AC Model



$$g_m = 2K_N (V_{gsQ} - V_{T_N}) = \boxed{2.23 mA/V}$$

$$r_o = \frac{V_M}{I_{dQ}} = \boxed{20k\Omega}$$

MOSFET (14)

(a) Unloaded Voltage Gain ($R_L \to \infty$) $A_{V_0} \triangleq \frac{v_o}{v_{gg}}$ | $R_L \to \infty$

KVL input loop:

$$v_{gg} = v_{gs} + (R_{S_R} /\!/ r_o) g_m v_{gs}$$

$$\Rightarrow v_{gs} = \frac{v_{gg}}{1 + (R_{S_R} /\!/ r_o) g_m}$$

KVL output loop:

$$v_o = (R_{S_R} /\!/ r_o)\, g_m v_{gs}$$

$$A_{V_0} = \frac{v_o}{v_{gg}} = \frac{(R_{S_R} /\!/ r_o) g_m}{1 + (R_{S_R} /\!/ r_o) g_m} = \boxed{0.802}$$

Note: for $(R_{S_R} /\!/ r_o) g_m \gg 1$ A_{V_0} will be slightly less than 1.0

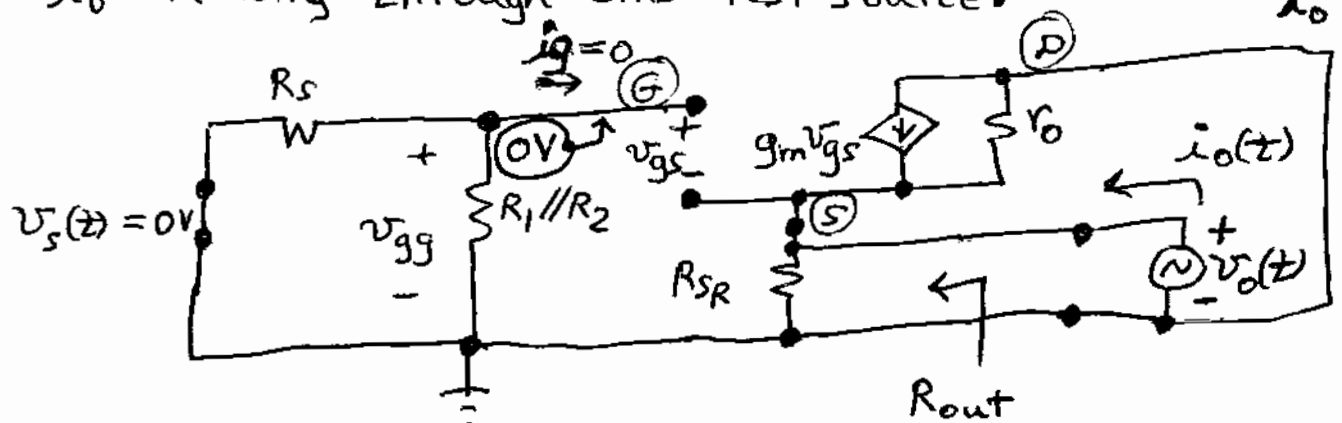
(b) Input Resistance R_{in}

By inspection $R_{in} = \boxed{R_1 /\!/ R_2} = \boxed{823.6\ k\Omega}$

(c) Output Resistance $R_{out} = \left.\frac{v_o}{i_o}\right|_{v_s(t)=0}$

Note that with MOSFET source follower R_{in} does NOT depend on R_L !!

Set $v_s(t) = 0$, place an ac test source $v_o(t)$ across output terminals and determine the current "i_o" flowing through this test source. Then $R_{out} = \frac{v_o}{i_o}$



Note the voltage on the gate wrt ground = 0V, since $v_s(t) = 0$ and $i_g = 0$ for a MOSFET. Also note R_{S_R} and r_o are "in parallel."

KCL: $i_o = v_o / (R_{S_R} // r_o) - g_m v_{gs}$

But $v_{gs} = V_g - V_s = 0V - v_o = -v_o$

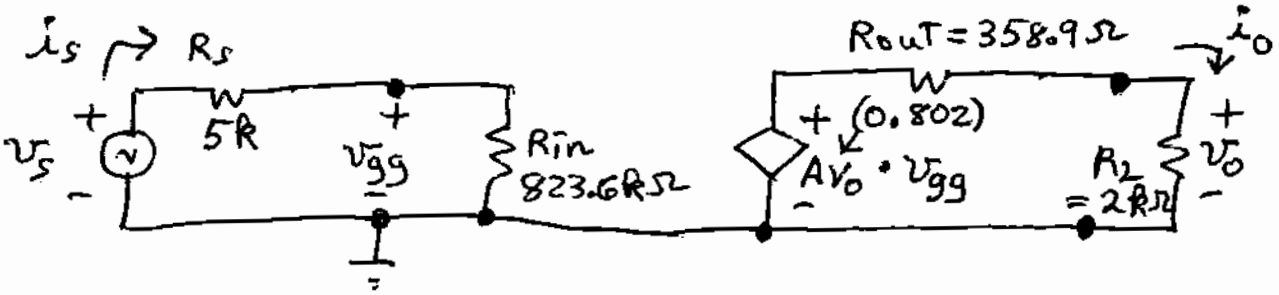
$$\therefore i_o = \frac{v_o}{(R_{S_R} // r_o)} + g_m v_o \Rightarrow v_o = \frac{(R_{S_R} // r_o) i_o}{1 + (R_{S_R} // r_o) g_m}$$

$$R_{out} = \boxed{\frac{(R_{S_R} // r_o)}{1 + (R_{S_R} // r_o) g_m}} = \boxed{358.9\,\Omega}$$

Note that with MOSFET "Source Follower" Rout does NOT depend on R_S!!

Note that if $(R_{S_R} // r_o) g_m >> 1$, then $R_{out} \approx \frac{1}{g_m} = 447\,\Omega$ (in this case.)

Overall Voltage Gain, Current Gain, Power Gain



$$A_V = \frac{v_o}{v_s} = \frac{R_{in}}{R_s + R_{in}} \cdot A v_o \cdot \frac{R_L}{R_L + R_{out}} = \boxed{0.676}$$

$$A_i = \frac{i_o}{i_s} = \frac{v_o / R_L}{v_s (R_s + R_{in})} = A_V \left(\frac{R_s + R_{in}}{R_L} \right) = \boxed{280.2}$$

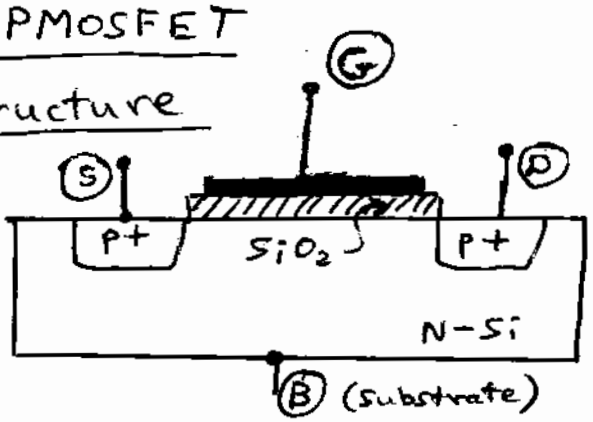
$$A_p = \frac{P_o}{P_i} = \frac{i_o \cdot v_o}{i_s \cdot v_s} = A_i \cdot A_V = \boxed{189.5}$$

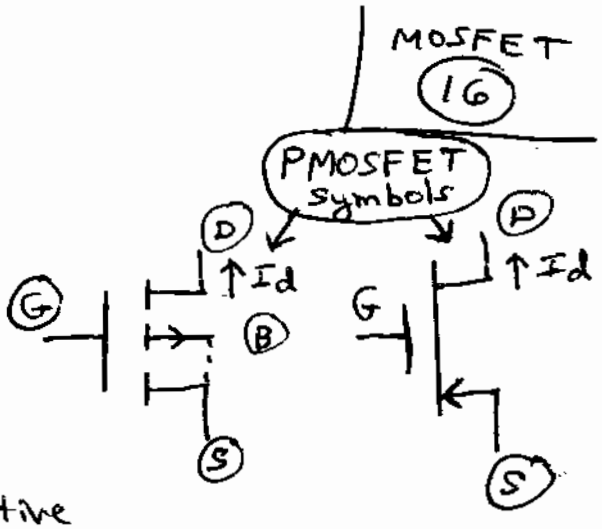
power gain in deciBels

$$(A_p)_{dB} = 10 \log(189.5) = \boxed{22.8\,dB}$$

8. PMOSFET

Structure





Now (D) is pin that is more negative than (S), which is opposite of NMOSFET

Now the threshold voltage is negative: $V_{Tp} = \begin{cases} -0.8 \\ \text{to} \\ -3V \end{cases}$

For $V_{gs} > V_{Tp}$ PMOSFET is cut off ($I_d = 0$)

For $V_{gs} < V_{Tp}$ PMOSFET is conducting in either ohmic (non-pinched off channel) or saturation (pinched-off channel) regions.

For non-pinched off channel we must require

$$V_{gs} - V_{ds} < V_{Tp} \quad \text{(Ohmic Region)}$$

where $$\boxed{I_d = K_p\left[2\left[V_{gs} - V_{Tp}\right]V_{ds} - V_{ds}^2\right]}$$

For pinched-off channel,

$$V_{gs} - V_{ds} > V_{Tp} \quad \text{(Saturation Region)}$$

where $$\boxed{I_d = K_p\left(V_{gs} - V_{Tp}\right)^2}$$

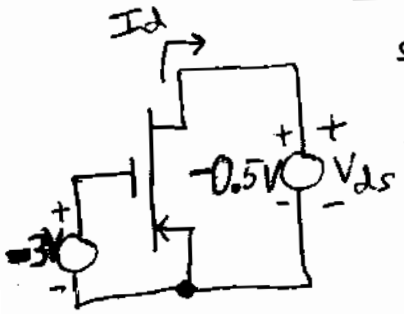
$$K_p = \frac{\mu_p \varepsilon_o \varepsilon_R \left(\frac{W}{L}\right)}{2\, t_{ox}} \; ; \quad \underset{\text{PSPICE}}{\text{"KP"}} = \frac{2L}{W} K_p$$

$$V_{TP} = \underset{\text{PSPICE}}{V_{TO}} = -2V \quad \text{(For example)}$$

Example Given PMOSFET with $V_{TP} = -2V$, $K_p = 2 \frac{mA}{V^2}$

And $V_{gs} = -3V$

(a) **If $V_{ds} = -0.5V$, find I_d**



$-2V$

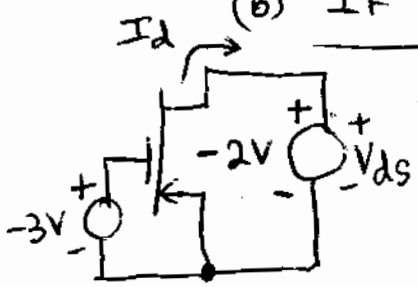
So $V_{gs} - V_{ds} = (-3V) - (-0.5V) = -2.5V < V_{TP}$

$\Rightarrow$ Ohmic

$$I_d = 2 \frac{mA}{V^2} \left[2 \left[-3 - (-2V) \right] (-0.5V) - (-0.5)^2 \right]$$

$$I_d = \boxed{1.5mA}$$

(b) **If $V_{ds} = -2V$, find I_d**



$-2V$

$V_{gs} - V_{ds} = (-3V) - (-2V) = -1V > V_{TP}$

$\Rightarrow$ Saturation

$$I_d = 2 \frac{mA}{V^2} \left[V_{gs} - V_{TP} \right]^2 = \boxed{2mA}$$

(c) **If $V_{ds} = -5V$, find I_d**

$-2V$

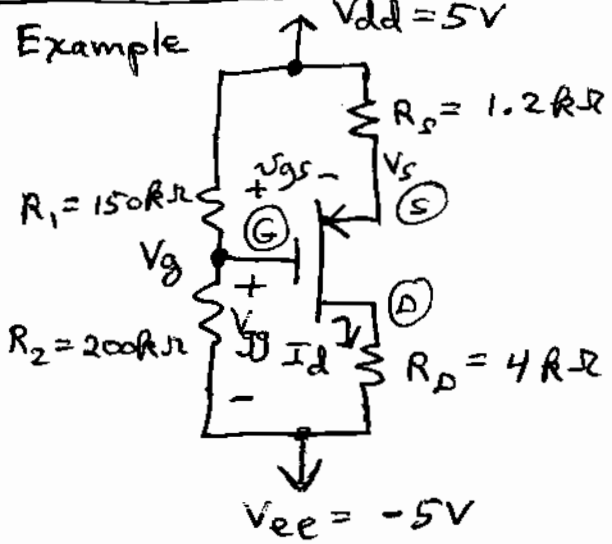
$V_{gs} - V_{ds} = -3 - (-5) = 2V > V_{TP}$

$\Rightarrow$ Saturation

$$I_d = 2 \frac{mA}{V^2} \left[V_{gs} - V_{TP} \right]^2 = \boxed{2mA}$$

PMOSFET DC Biasing — Find Q-pt

Example



$V_{Tp} = -1V$

$K_p = 0.25 \frac{mA}{V^2}$

$$V_g = (V_{dd} - V_{ee})\left(\frac{R_2}{R_1+R_2}\right) + V_{ee} = 0.7143\ V$$

$$V_{gs} = V_g - \underbrace{(V_{dd} - K_p(V_{gs} - V_{Tp})^2 R_s)}_{V_s}$$

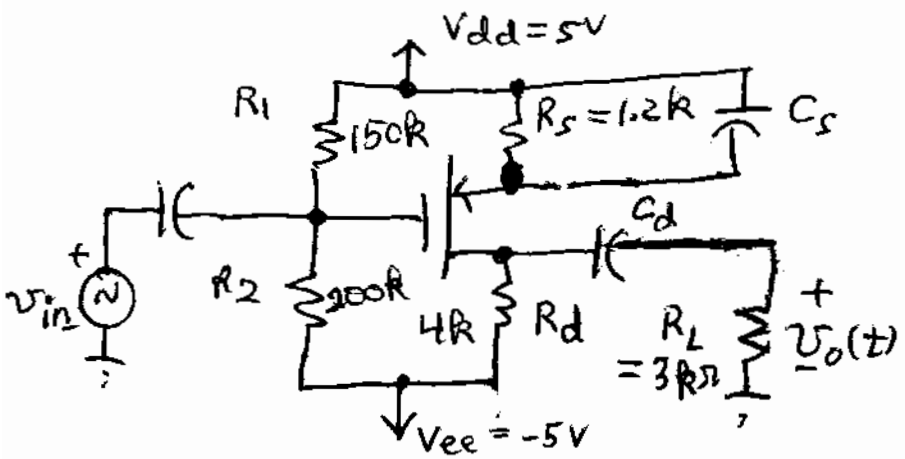
$\Rightarrow V_{gs} =$ **$-3.0387\ V$** or $4.3720\ V$ (Reject $V_{gs} > V_{Tp}$)

$$I_d = K_p(V_{gs} - V_{Tp})^2 = \boxed{1.039\ mA}$$

$$V_D = I_d R_d + V_{ee} = -0.844V$$

$$V_{DS} = V_D - V_S$$

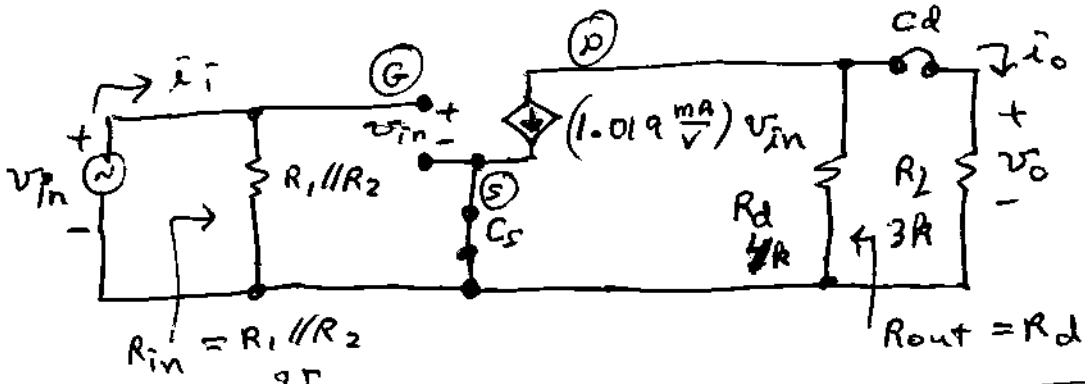
$$V_{DS} = -0.844 - (V_{dd} - K_p(V_{gs} - V_{Tp})^2 R_s) = \boxed{-4.59V}$$



$$g_m = |2K_p(V_{gsQ} - V_{Tp})|$$

$$= 1.019\ mA/V$$

AC Model



$$A_V = \frac{v_o}{v_{in}} = -(1.019\text{mA/V})(R_d // R_L) = \boxed{-1.74}$$

$$R_{in} = R_1 // R_2 = 85.71\,\text{k}\Omega$$

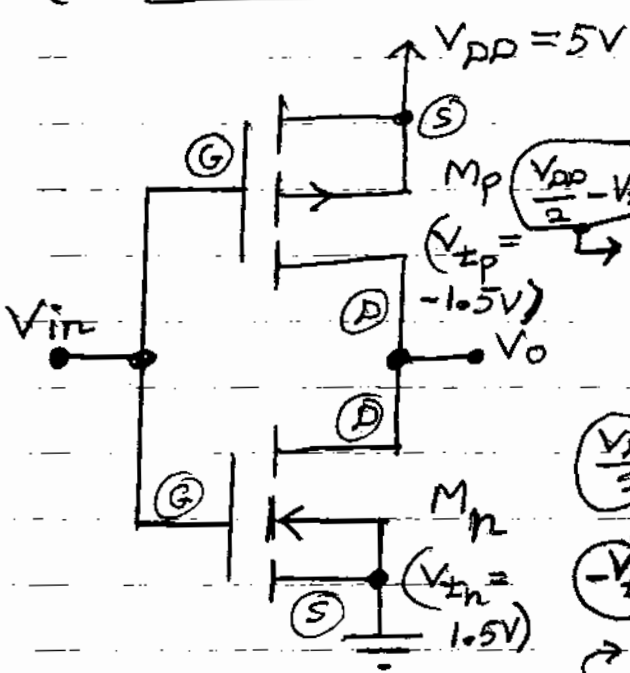
$$A_I = \frac{v_o/R_L}{v_{in}/R_{in}} = A_V\left(\frac{R_{in}}{R_L}\right) = (-1.74)\left(\frac{85.71\text{k}\Omega}{3\text{k}}\right)$$

$$= \boxed{-49.9}$$

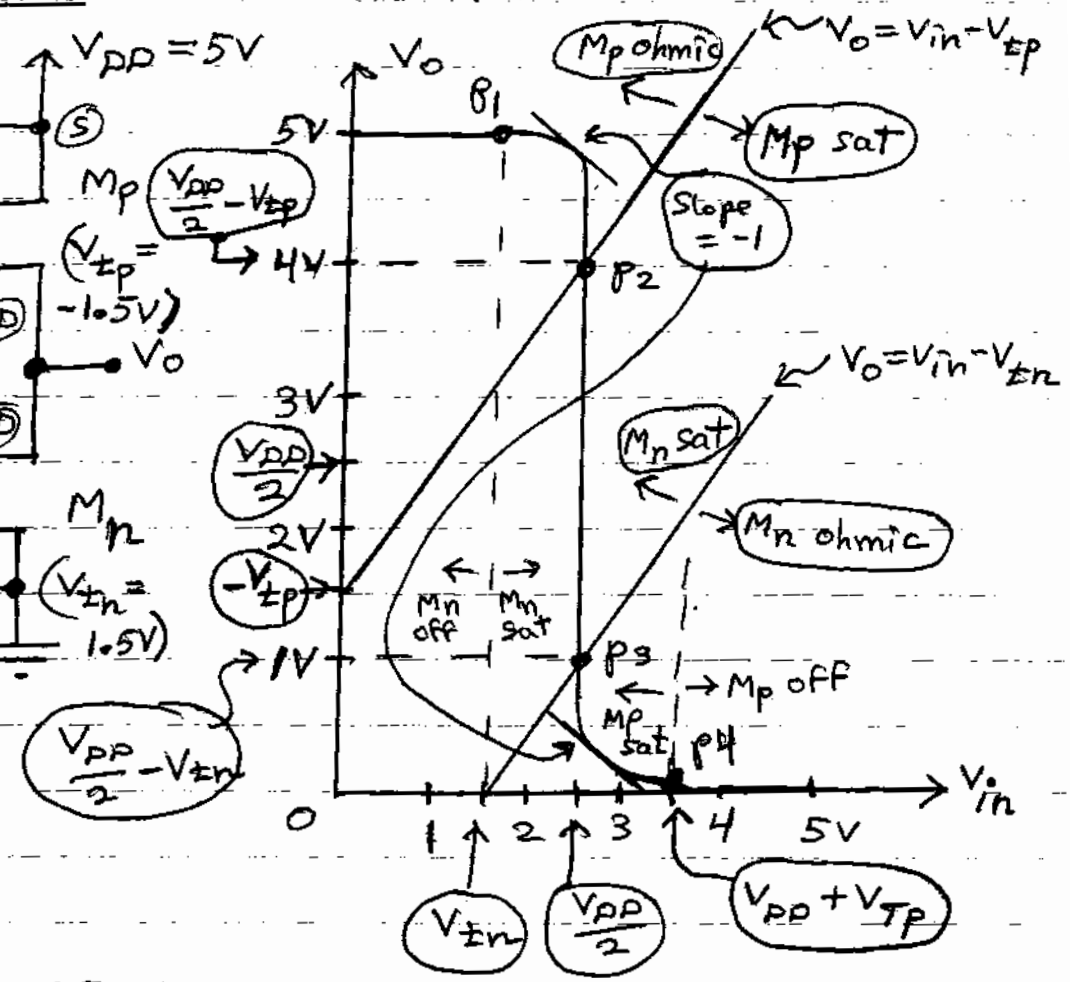
$$A_P = \frac{P_o}{P_i} = \frac{v_o \cdot i_o}{v_i \cdot i_i} = A_V \cdot A_I = \boxed{87.24}$$

9. CMOS Logic

(a) CMOS Inverter



(b) VTC



Assume PMOSFET M_p has $V_{T_P} = -1.5V$, M_N has $V_{T_N} = +1.5V$

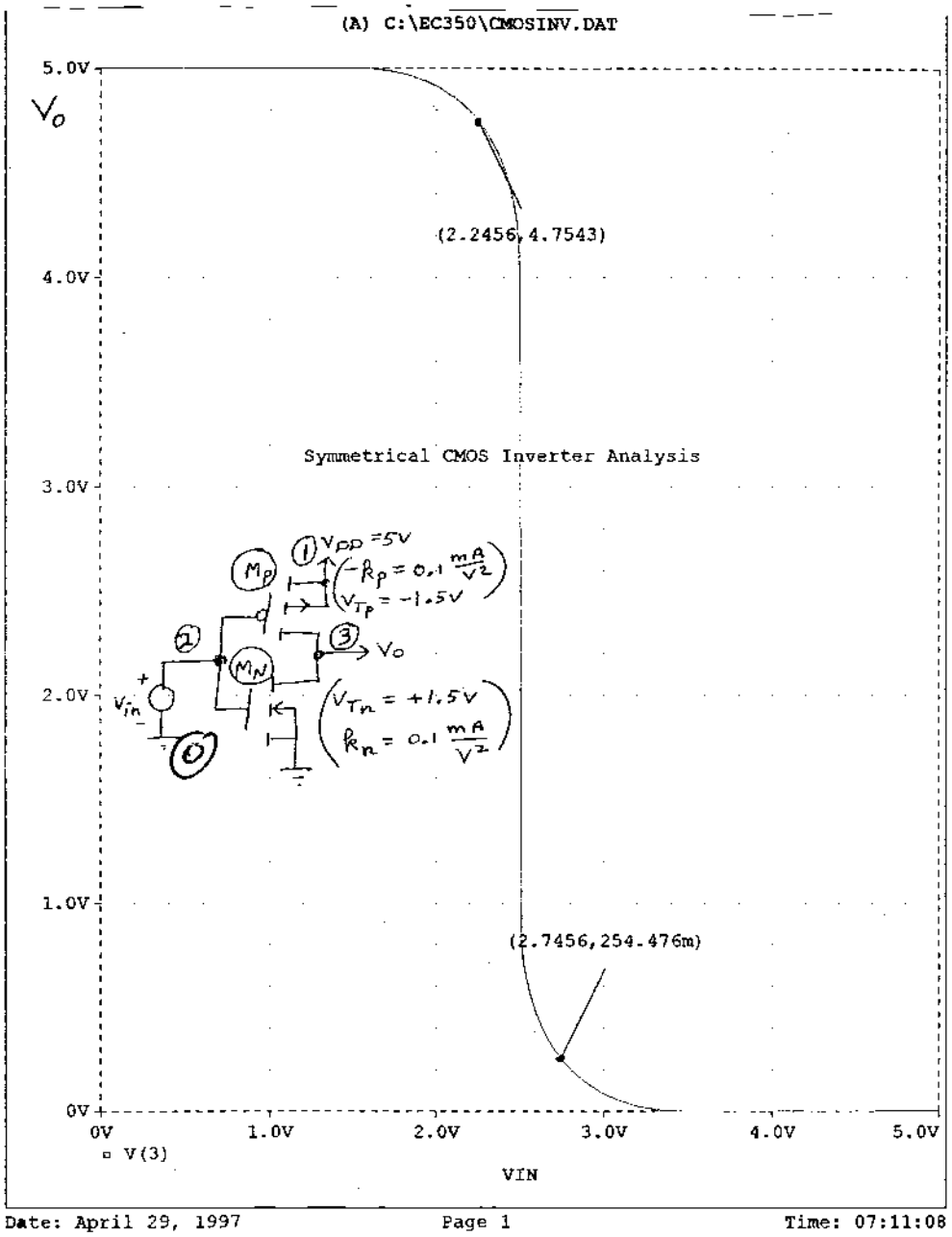
Then

(i) For $V_{in} = 0V$ (Logic Low), $V_{gs}(M_p) = -5V < V_{TP} \Rightarrow M_p$ ON
$V_{gs}(M_N) = +0V < V_{TN} \Rightarrow M_N$ OFF
$\Rightarrow V_o = +5V$ (Logic High)

(ii) For $V_{in} = 5V$ (Logic High), $V_{gs}(M_p) = 0V > V_{TP} \Rightarrow M_p$ OFF
$V_{gs}(M_N) = 5V > V_{TN} \Rightarrow M_N$ ON
$\Rightarrow V_o = 0V$ (Logic Low)

(iii) For $1.5 < V_{in} < 3.5V$ ("Forbidden" input voltage range)
$V_{gs}(M_p) < V_{TP} \Rightarrow M_p$ ON
$V_{gs}(M_N) > V_{TN} \Rightarrow M_N$ ON
$\Rightarrow V_o$ in Transition between Logic levels

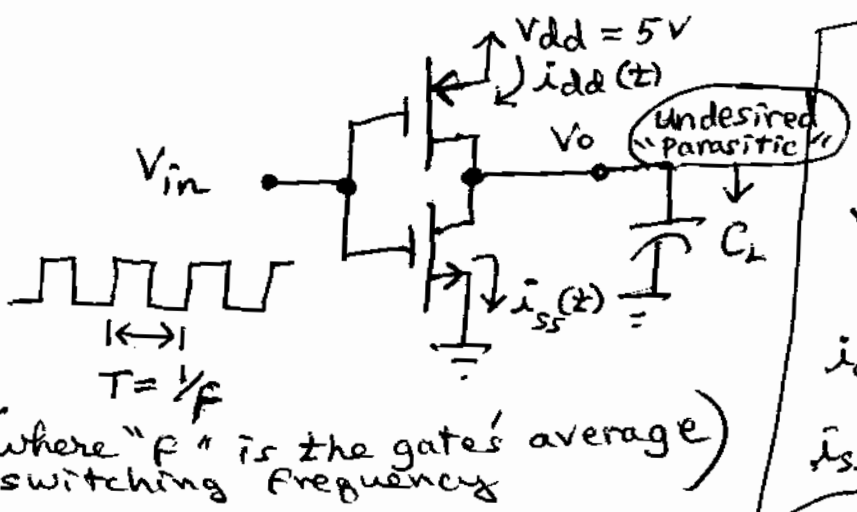
CMOS Inverter Voltage Transfer Curve
SPICE (DC-sweep) simulation



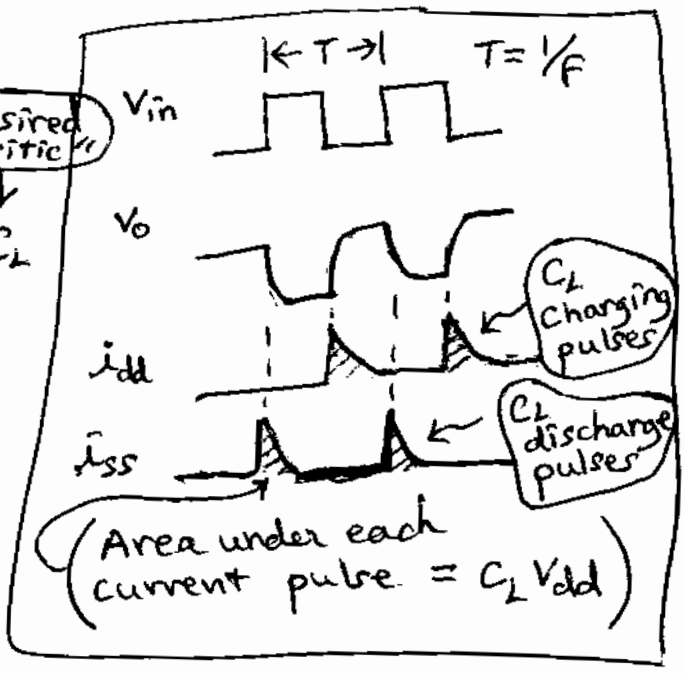
(b) CMOS Average DC Power Consumption

Since the PMOSFET is <u>off</u> during logic 0 input and the NMOSFET is <u>off</u> during logic 1 input. The dc power consumption of a CMOS gate that is driving a <u>constant</u> logic level is $\approx \underline{\underline{0}}$!

However, as the CMOS gate switches the output from $0V \rightarrow V_{dd}(=5V)$, the capacitance at the output of the gate must be charged by current flowing through the V_{dd} dc power supply. Since $C \triangleq \frac{Q}{V}$, the charge supplied each switching cycle must be $Q = C_L \cdot V_{dd}$



(where "f" is the gate's average switching frequency)



Thus $Q = CV$ coulombs flow from the V_{dd} power source every "T" $(= 1/f)$ seconds and thus

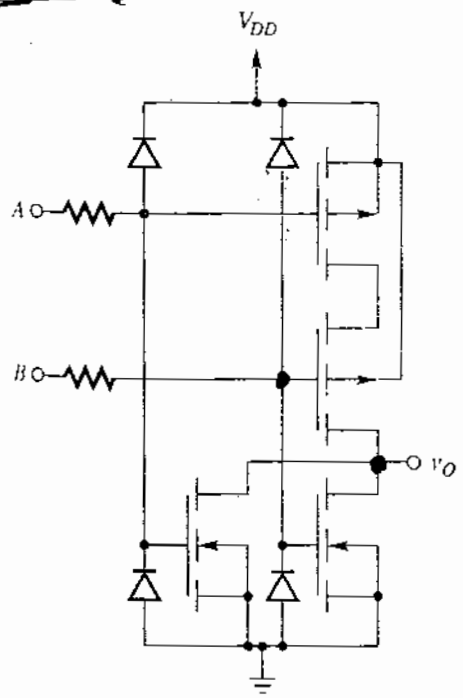
$$I_{dd_{Avg}} = \frac{Q}{\Delta T} = \frac{CV}{T} = fCV$$

The average dc power "consumed" by the CMOS gate is $P_{Avg} = V_{dd} \cdot I_{dd_{Avg}} = \boxed{f C_L V_{dd}^2}$ ← Thus avg dc power consumption $\propto$ "f"

(C) CMOS NAND & NOR Gates

(diodes and input resistors form an "electrostatic discharge" (ESD) protection circuit that "clips" the input voltages to the range of (V_{DD}+0.7v) to (0−0.7v), thereby protecting the MOSFETs in the event that electrostatic charge is allowed to build up on either input.)

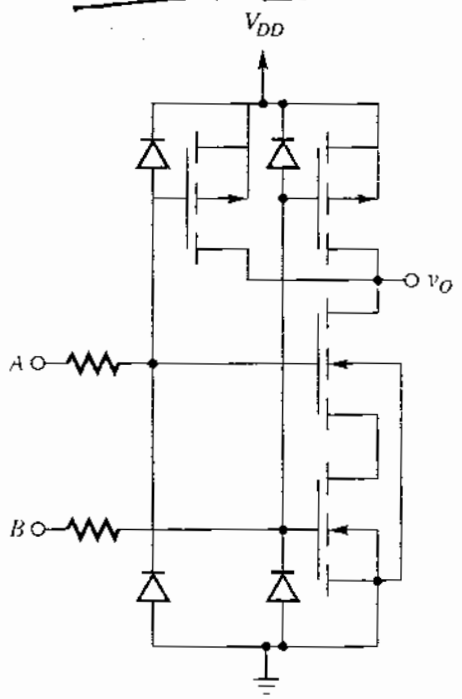
CMOS NOR Gate



(a)

A	B	V_o
0	0	1
0	1	0
1	0	0
1	1	0

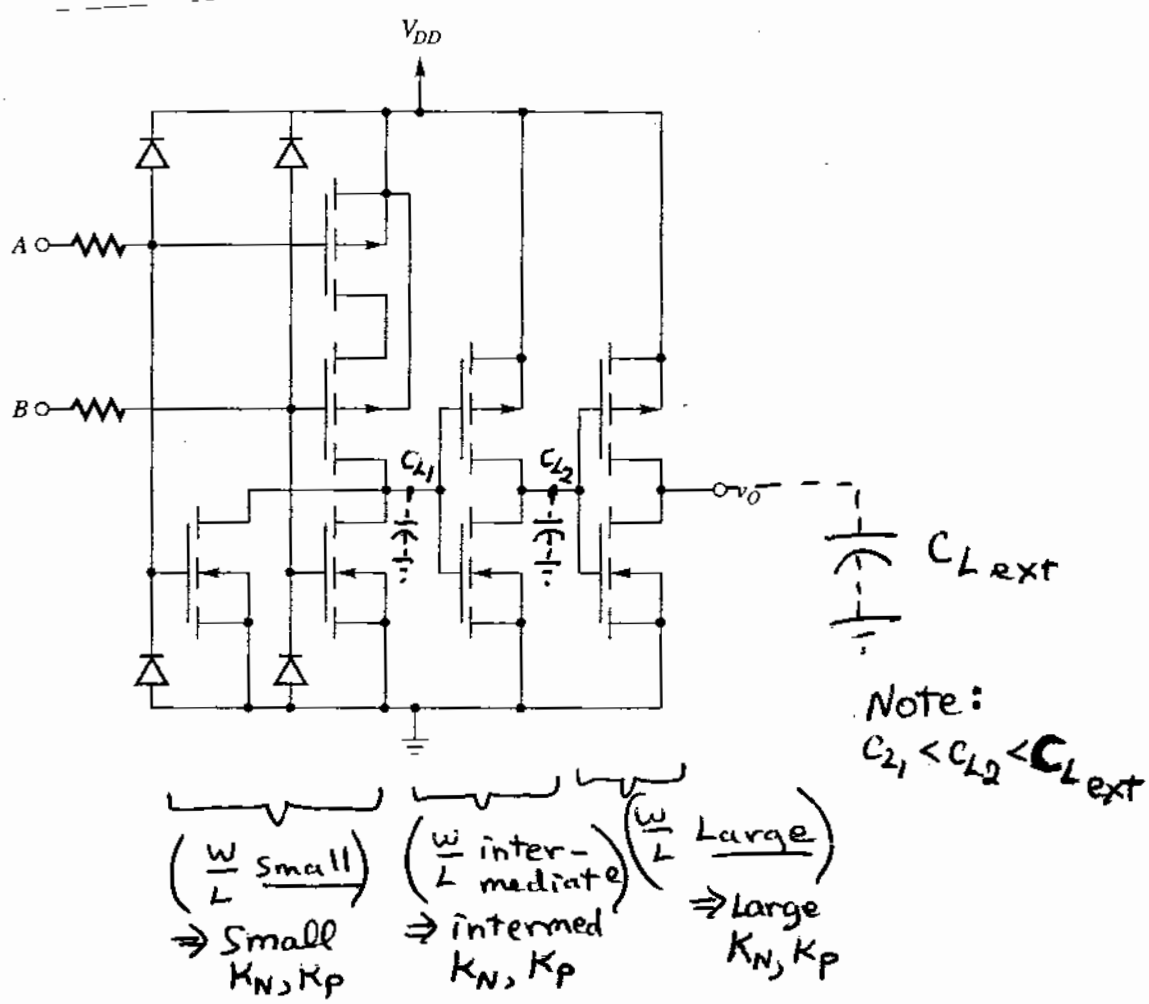
CMOS NAND Gate



(b)

A	B	V_o
0	0	1
0	1	1
1	0	1
1	1	0

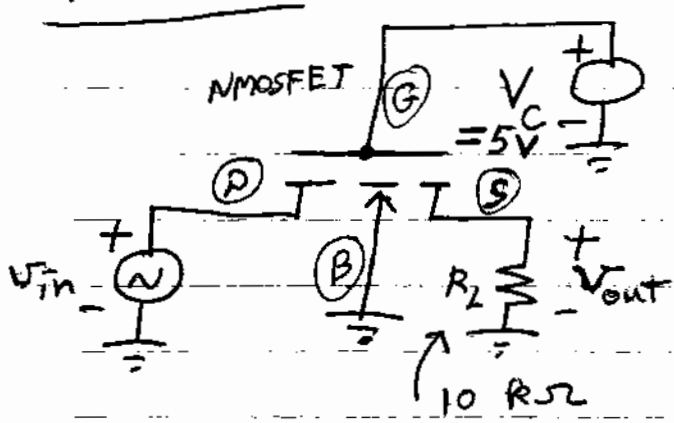
(d) Buffered CMOS NOR Gate (74HC02)

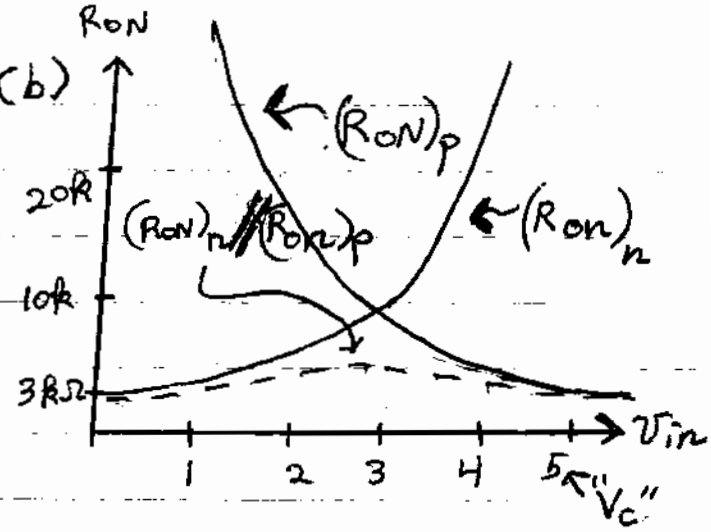


L is usually fixed and W is varied in a VLSI design. Buffering circuits are typically applied to VLSI IC output pins to allow a relatively large external parasitic (unwanted) load capacitance ($C_{L\,ext}$) to be driven (rapidly high or low). The internal NOR gate is made with very small MOSFETs with small "W", so "C_{L1}" for that small NOR gate is small and the gate is fast, but $K_N = K_P$ or $\frac{W}{L}$ so the MOSFET conduction parameters are also small. To drive the large $C_{L\,ext}$, we pass through to CMOS inverters with increasing W/L ratios that build up K_N and K_P, permitting $C_{L\,ext}$ to be switched

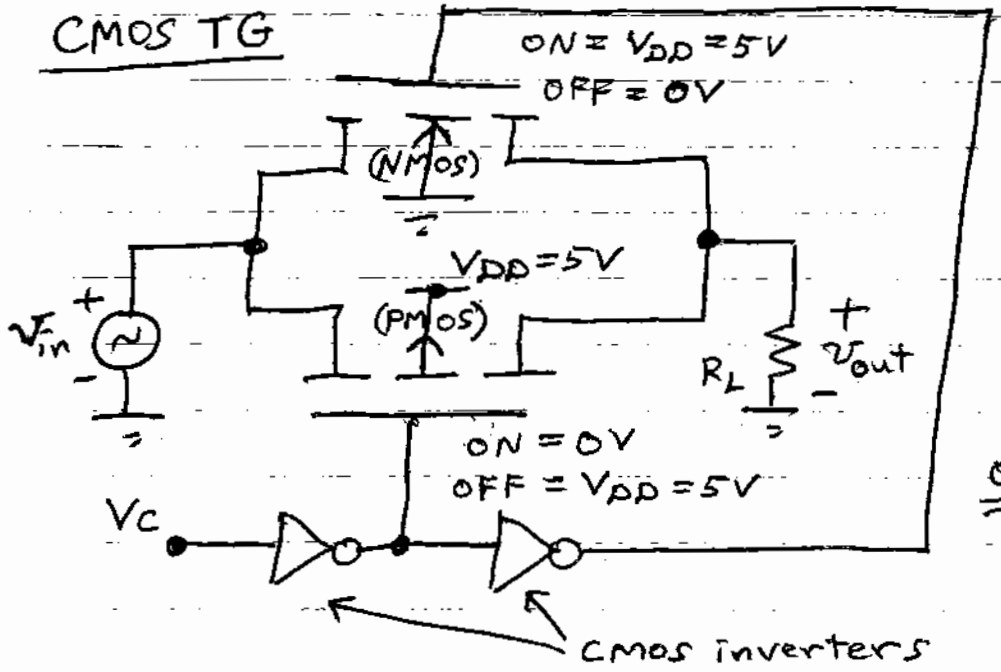
10. NMOS and CMOS Analog Switches "Transmission Gates" (TG)

NMOS TG

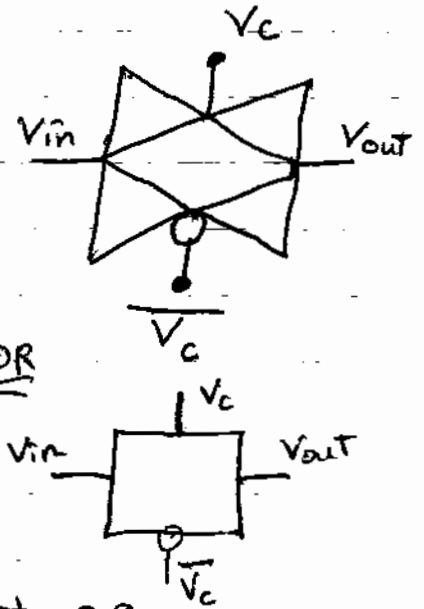




CMOS TG



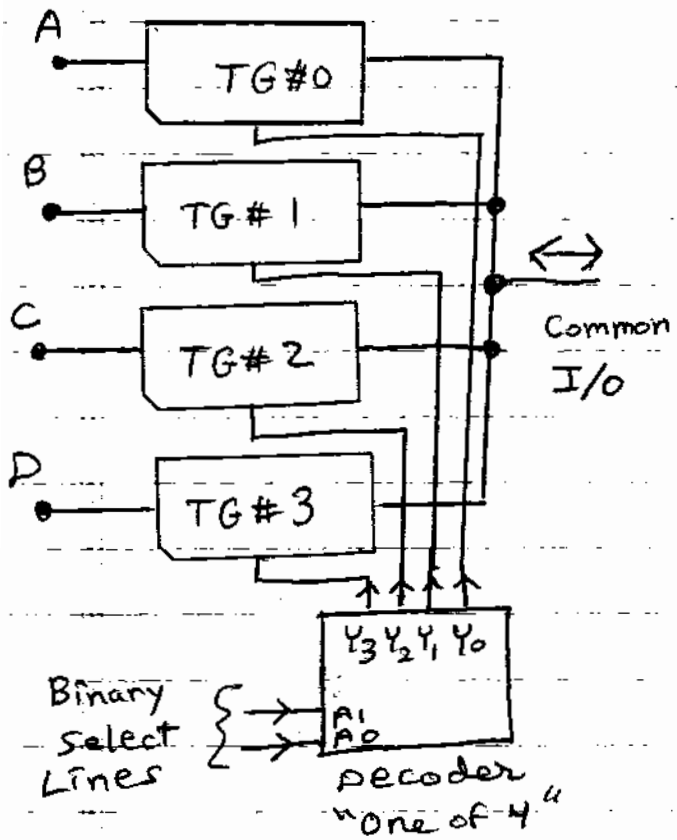
(d) CMOS TG Symbols



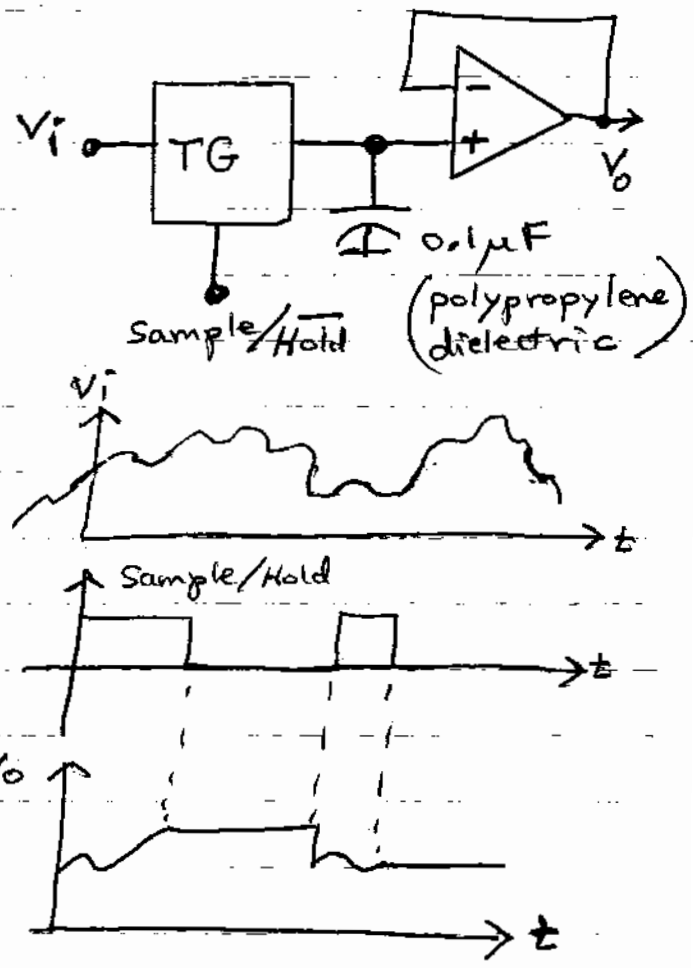
Consider the NMOS TG. Note that as the analog input $v_{in}(t)$ varies over the range of 0V → 5V, as it approaches $V_C = 5V$, its "ON" resistance $(R_{ON})_n$ increases to an unusable level. However the CMOS TG has $(R_{ON})_p$ and $(R_{ON})_N$ in parallel, so its ON resistance remains low over the entire input range !!

CMOS TG Applications

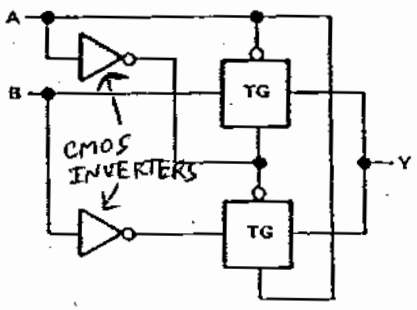
(a) Analog Multiplexer/Demultiplexer



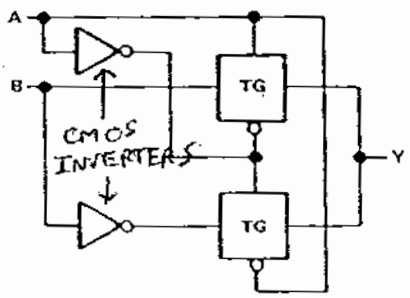
(b) Sample/$\overline{\text{Hold}}$ CKt

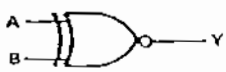


(c) Efficient design of XOR via TGs



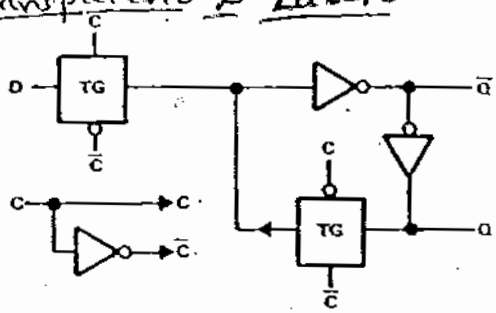
A B	Y
L L	L (= B)
L H	H (= B)
H L	H (= $\bar{B}$)
H H	L (= $\bar{B}$)

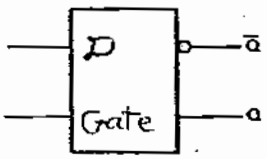




A B	Y
L L	H (= $\bar{B}$)
L H	L (= $\bar{B}$)
H L	L (= B)
H H	H (= B)

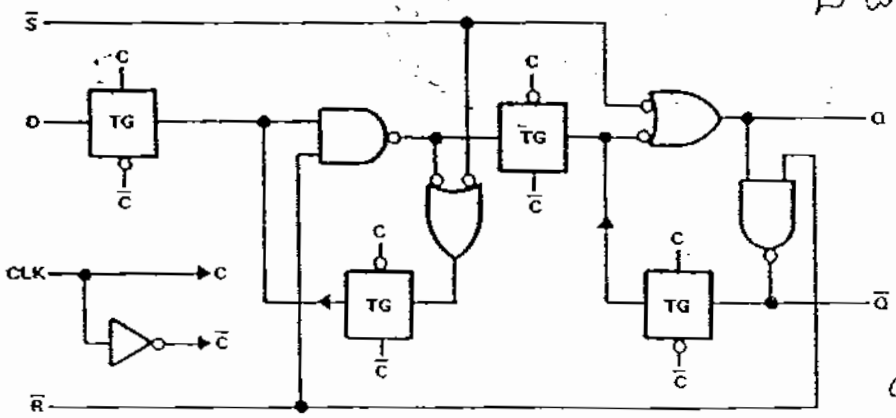
(d) Transparent D Latch

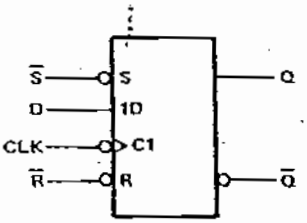




while Gate High, Q = D
when Gate falls,
Q holds value on
D when Gate fell.

(e) Falling Edge D Flip-Flop



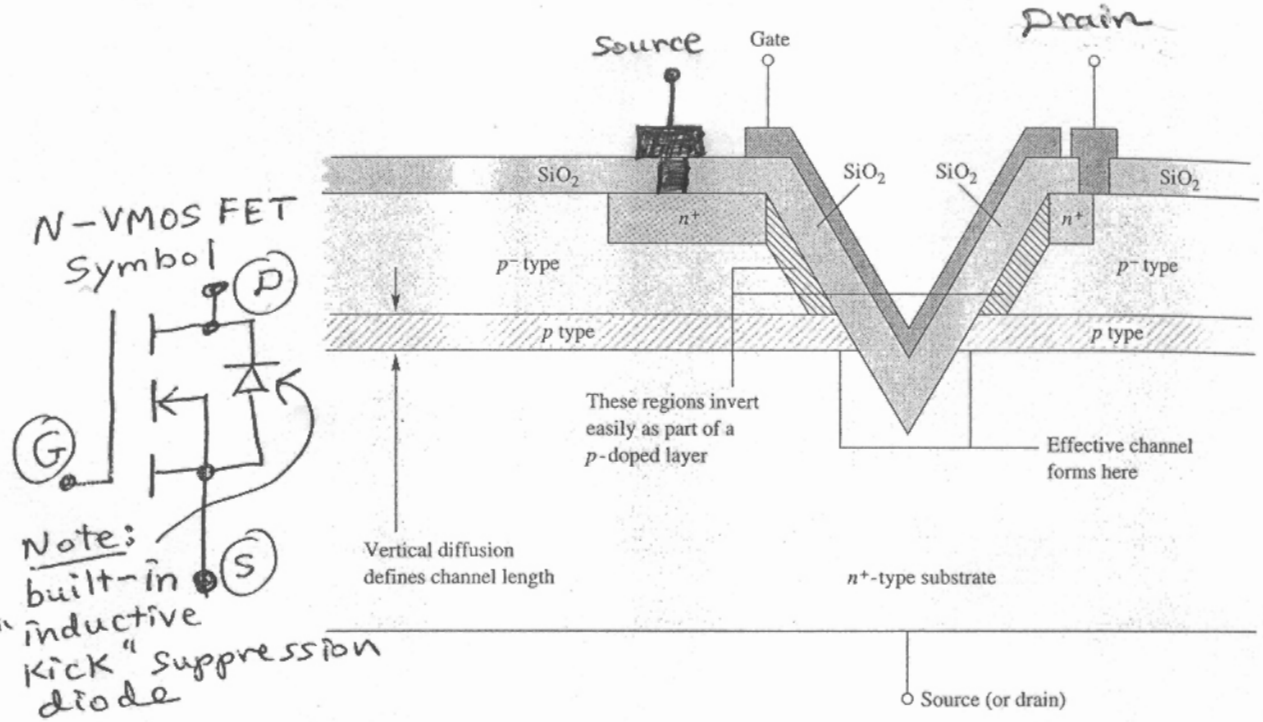


Negative-Edge-Triggered D-Type Flip-Flops

Q changes to current value of D only when CLK falls.

11. Electrical Symbol and Cross-sectional View of Power Vertical MOSFET (VMOS) Device

We have several of these in our instrument room (IR540)



N-VMOS FET Symbol

Note: built-in "inductive kick" suppression diode

Switching Application: