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Introduction to Bipolar Junction Transistors

(Read Chapter 3 of Text)

Bipolar Junction Transistor

- Current-controlled current source
- Made by sandwiching thin N-type Si between two P-type Si (PNP BJT)
- Or by sandwiching thin P-type Si between two N-type Si (NPN BJT)
- Leads called Base (B), Collector (C) and Emitter (E). Control current "I_B" flows from B to E. Resulting current "I_C" is "pumped" from C to E.

NPN and PNP BJTs

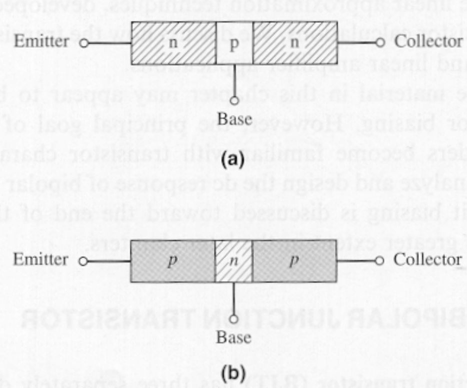


Figure 3.1 Simple geometry of bipolar transistors: (a) npn and (b) pnp

Integrated Circuit NPN BJT

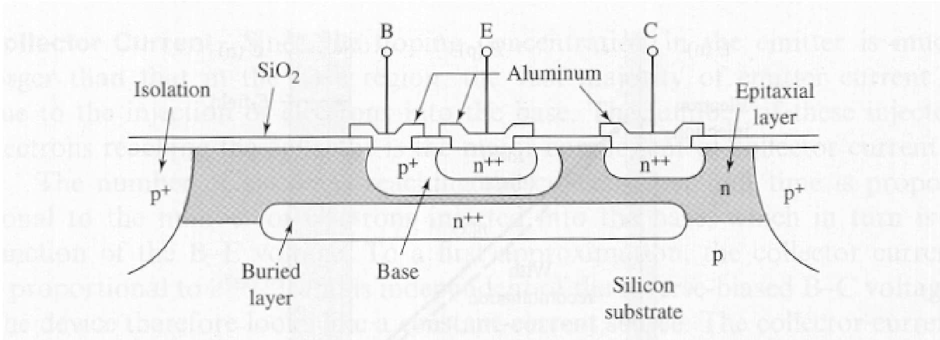


Figure 3.2 Cross section of a conventional integrated circuit npn bipolar transistor

The previous slide implied that the C and E leads are interchangeable, but it can be seen above that the emitter (E) is doped more heavily (n++) than the collector region (n), and the collector (C) surrounds the base region (p+), while E is a small button. The doping levels for E, B, and C regions are 10^{19}, 10^{17} and 10^{15} cm^{-3}, respectively. Note the aluminum contact to the collector "n-type Si" region is made using an "n++" diffusion so that the contact is "ohmic" rather than a rectifying Schottky diode.

NPN BJT is biased in "Forward Active" mode when B-E pn junction is forward biased and B-C pn junction is reverse biased.

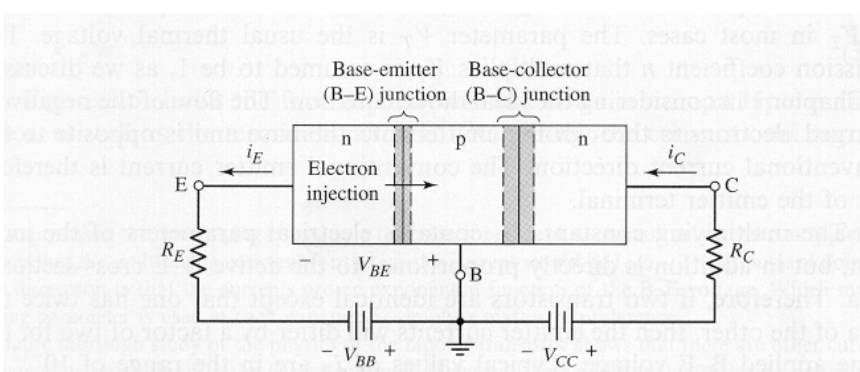


Figure 3.3 An npn bipolar transistor biased in the forward-active mode

Electron Current in Forward-Active NPN BJT

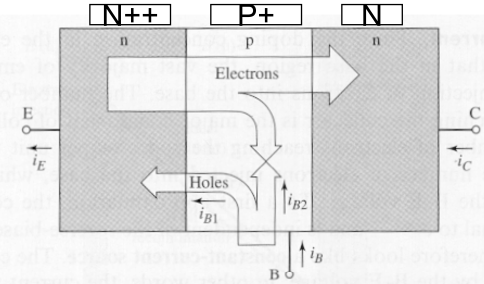


Figure 3.5 Electron and hole currents in an npn transistor biased in the forward-active mode

Electrons from the highly-doped emitter “n++” region are injected into base region through the forward-biased BE junction. They diffuse through the VERY THIN base region, with only a few of these electrons having a chance to recombine with holes in the thin “p+” base region. The vast majority of the injected electrons (perhaps $\alpha \approx 0.99$ of the injected electrons) diffuse to the edge of the base region near the reverse-biased BC junction, where the intense electric field associated with the reverse-biased BC junction (directed from N to P regions) sweeps these electrons into the “n” collector region, where they constitute collector current. The remaining “$1-\alpha$”$= 1 - 0.99 \approx 0.01$ of the injected electrons that recombine with holes in the base region constitute a portion of the small base current “Ib1”.

Hole Current in Forward-Active NPN BJT

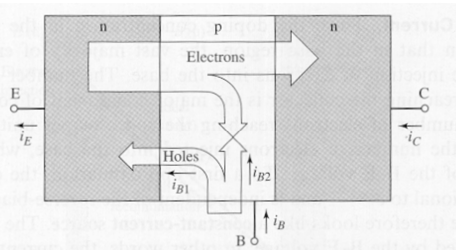


Figure 3.5 Electron and hole currents in an npn transistor biased in the forward-active mode

We shall see that the electron current diffusing across the forward-biased B-E junction from E to B regions, as discussed on the previous slide, results in desirable transistor action. However, the hole current that flows from B to E region adds an UNDESIRED contribution “Ib2” to the total base current, Ib = Ib1 + Ib2. We desire that the total base current “Ib” be as small as possible for a given collector current “Ic”. This results in a “forward current transfer ratio” (current gain) $\beta_F =$ Ic / Ib that is as large as possible. The undesired hole current component of Ib (Ib2) is made negligibly small by doping the E region heavily (n++) and the base region about 100 times less heavily than the B region (p+).

Relationship between Emitter, Base, and Collector Current in a Forward-Active BJT

- $I_E = I_s*\exp(V_{BE}/V_T)$, since the BE junction is forward-biased. (Note $\eta = 1$ for IC BJTs.)
- $I_C = \alpha*I_E$, because $\alpha \approx 0.99$ of the electrons injected into the THIN base region diffuse across the base and get swept across the reverse-biased BC junction.
- $I_B = (1-\alpha)*I_E$, because the remaining $(1-\alpha) \approx 0.01$ of the electrons recombine with holes in the base region.

Relating β to α

- α_F, the "forward current transfer ratio" is defined as the ratio of collector to emitter current in a forward-active BJT

  Note: $I_C/I_E = \alpha_F*I_E / I_E = \alpha_F$
- β_F, the "transistor current gain" is defined as the collector current divided by the controlling base current in a forward-active BJT.
- Note $\beta_F = I_C/I_B = \alpha_F*I_E / (1-\alpha_F)*I_E = \alpha_F/(1-\alpha_F)$
- Thus if $\alpha_F = 0.99$, $\beta_F = 0.99/(1-0.99) = 99$
- The subscript "F" is often dropped, if it is clear that we are talking about a forward-active BJT.

NPN BJT in "Common Emitter" Configuration

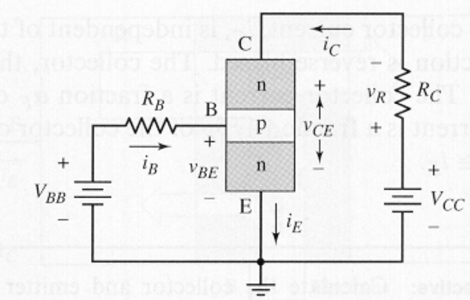


Figure 3.6 An npn transistor circuit in the common-emitter configuration

Voltage source V_{BB} forward-biases BE junction (assuming V_{BB} > 0.7V), making $V_{BE} \approx 0.7$ V.

Voltage source V_{CC} reverse-biases BC junction. Thus BJT is biased into its "forward-active" region, and

$I_B = (V_{BB} – 0.7V)/R_B$, $I_C = \beta_F I_B$, and $I_E = I_C + I_B = (\beta_F+1) I_B$

Operating Modes of NPN BJT

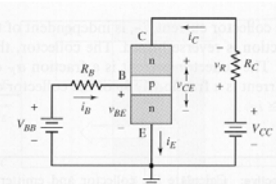


Figure 3.6 An npn transistor circuit in the common-emitter configuration

1. If V_{BB} < 0.7 V, both BE and BC junctions are OFF, and BJT is "***cut off***". No currents flow in a cut off BJT $I_C = I_E = I_B = 0$. The terminals of the BJT are essentially "open-circuited".
2. If V_{BB} > 0.7 V, V_{CC} > 0.1 V, BE junction is forward-biased, and BC junction is reverse-biased. So BJT is ***forward active***, where $I_C = \beta I_B$.
3. If, while in forward-active mode, V_{BB} is increased to a point where $V_{CE} = V_{CC} – \beta_F I_B R_C$ falls below about 0.1V, V_{BE} = 0.7V (on hard) and $V_{BC} = V_{BE} – V_{CE}$ = 0.7V – 0.1V = 0.6V, and thus the BC junction turns on (lightly). Under this condition the BJT is said to be ***saturated***. I_C no longer = $\beta_F I_B$. Instead, the BE junction acts like a 0.7 V battery and the BC junction acts like a 0.6 V battery.

4. Reverse Active Mode (BC fwd-biased, BE rev-biased)

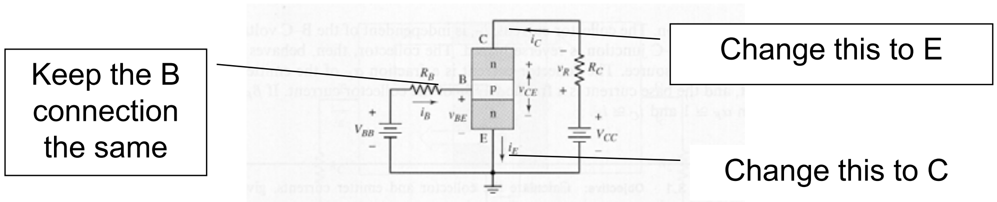


Figure 3.6 An npn transistor circuit in the common-emitter configuration

- If C and E terminals are interchanged in the circuit above, it would at first seem that the circuit will function exactly as it did before due to the apparent symmetry of the BJT. Now the BC junction will be forward-biased and the BE junction will be reverse-biased.
- However, we learned earlier that a modern BJT is NOT symmetric, since the C and E regions are different shape, and the doping level in the E region is much higher (n++) than the doping level in the C region (n).
- Thus with C and E interchanged, the BJT operates in ***reverse active*** mode, which is similar to forward active mode, except the roles of I_E and I_C have been interchanged, and now the undesired hole current component of Ib (Ib2) is much larger and more injected electrons recombine in the base region, thereby reducing the forward transfer current ratio well below 1. Now $\alpha_R \sim 0.5$, and now $\beta_R = \alpha_R/(1-\alpha_R) \sim 1$.
- Now $I_E = \beta_R I_B$ and $I_C = (\beta_R + 1)I_B$, since the roles of C and E are reversed.

Electron and Hole Currents in a Forward-Active PNP BJT

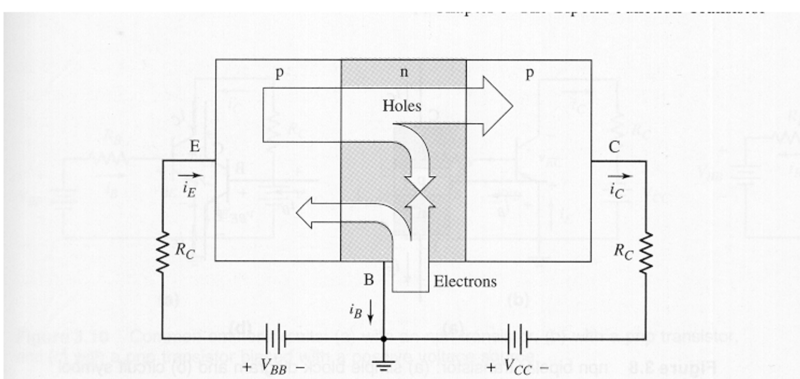


Figure 3.7 Electron and hole currents in a pnp transistor biased in the forward-active mode

Forward Active PNP BJT has SAME equations as before, just opposite current and voltage polarities! As before, BE junction is forward biased and BC junction is reverse biased. Now $(V_{EB})_{on} = 0.7$ V.

$$Ic = \alpha_F * I_E \qquad I_C = \beta_F I_B \qquad I_E = (\beta_F + 1)I_B$$

NPN and PNP BJT Symbols

Note that emitter arrow indicates reference direction of emitter current, I_E

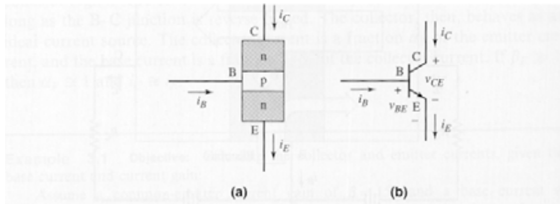


Figure 3.8 npn bipolar transistor: (a) simple block diagram and (b) circuit symbol

Figure 3.9 pnp bipolar transistor: (a) simple block diagram and (b) circuit symbol

Summary of NPN and BJT Fwd Active Equations

Table 3.1 Summary of the bipolar current–voltage relationships in the active region

npn	pnp
$i_E = I_S e^{v_{BE}/V_T}$	$i_E = I_S e^{v_{EB}/V_T}$
$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{BE}/V_T}$	$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{EB}/V_T}$
$i_B = \dfrac{i_C}{\beta_F} = \dfrac{\alpha_F I_S}{\beta_F} e^{v_{BE}/V_T}$	$i_B = \dfrac{i_C}{\beta_F} = \dfrac{\alpha_F I_S}{\beta_F} e^{v_{EB}/V_T}$

For both transistors

$i_C = \beta_F i_B$	$\alpha_F = \dfrac{\beta_F}{1+\beta_F}$
$i_E = (1+\beta_F) i_B$	
$i_C = \left(\dfrac{\beta_F}{1+\beta_F}\right) i_E = \alpha_F i_E$	$\beta_F = \dfrac{\alpha_F}{1-\alpha_F}$

Common-Emitter NPN and PNP BJT Circuits

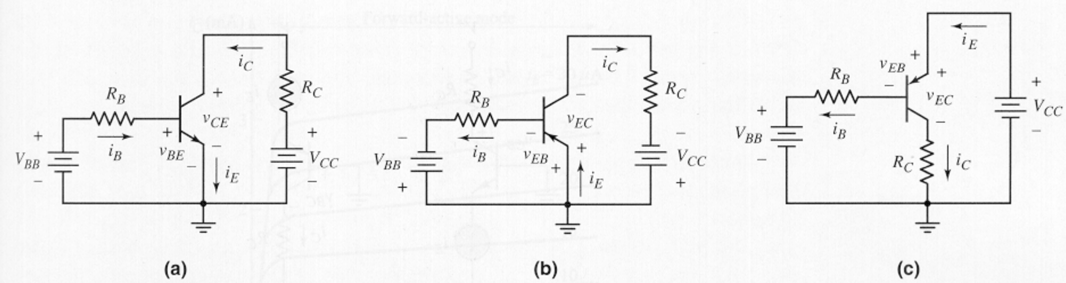


Figure 3.10 Common-emitter circuits: (a) with an npn transistor, (b) with a pnp transistor, and (c) with a pnp transistor biased with a positive voltage source

Typical I vs V "Family of Curves" for the Common-Emitter NPN BJT Circuit

(Ideally, each curve should be horizontal, so $I_C = \beta_F I_B$ for any VCE > 0.1V)

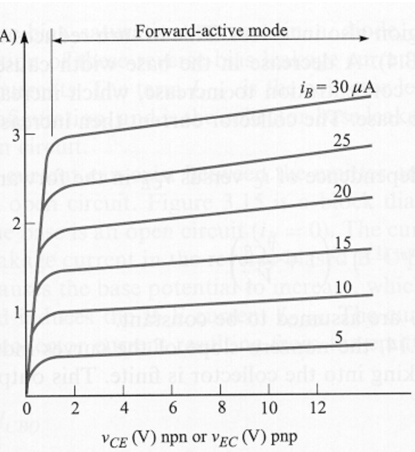


Figure 3.13 Transistor current–voltage characteristics of the common-emitter circuit

Non-Ideality Parameters for the BJT: V_A and BV_{CEO}

Early Voltage (Base-Width Modulation) Parameter, V_A

$50\text{ V} < V_A < 300\text{ V}$

$I_C = \alpha_F I_S \exp(V_{BE}/V_T)(1+V_{CE}/V_A)$

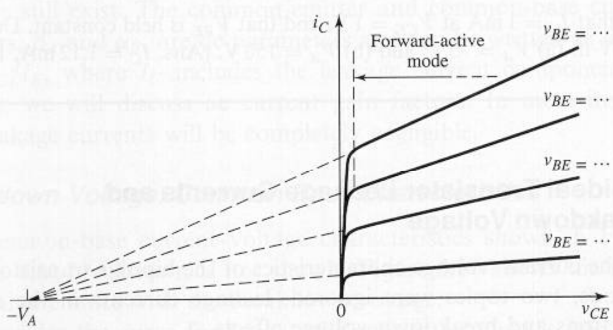


Figure 3.14 Current–voltage characteristics for the common-emitter circuit, showing the Early voltage

[3]Even though the collector current is essentially equal to the emitter current when the B–C junction becomes slightly forward biased, as was shown in Figure 3.12, the transistor is said to be biased in the forward-active mode when the B–C junction is zero or reverse biased.

BV_{CEO} Breakdown Voltage Parameter

Vce gets so large that the reverse-biased BC junction breaks down, allowing Ic to increase dramatically, losing the $I_C=\beta_F I_B$ amplifying effect.

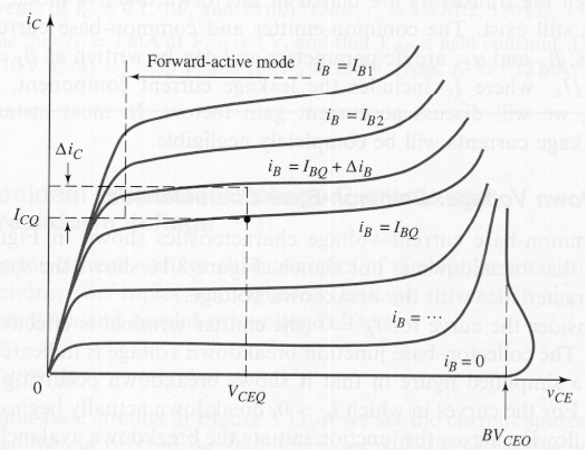


Figure 3.17 Common-emitter characteristics showing breakdown effects

DC Equivalent Forward-Active Model of NPN BJT

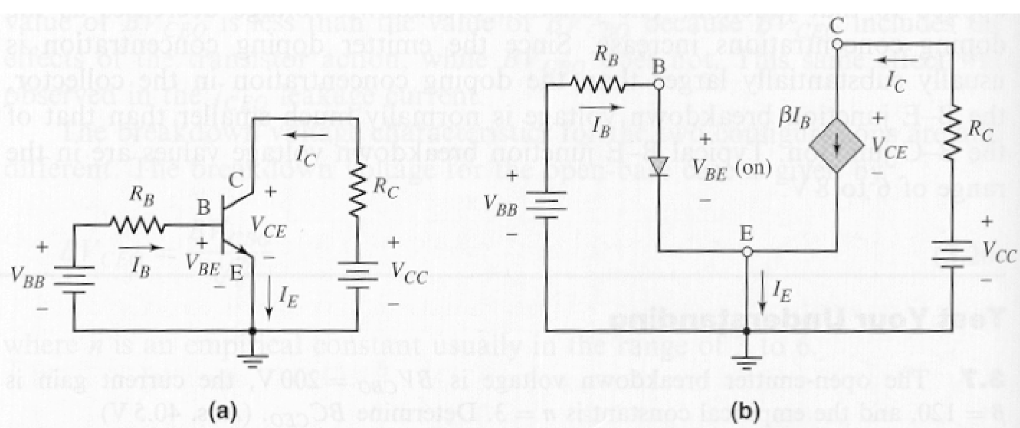


Figure 3.18 (a) Common-emitter circuit with an npn transistor and (b) dc equivalent circuit, with piecewise linear parameters

NPN BJT DC Analysis

($\beta_F = 200$, $V_{BEON} = 0.7$ V, $V_{CESAT} = 0.1$V)

Since V_{BB} > VBEon, assume BJT is Forward Active.

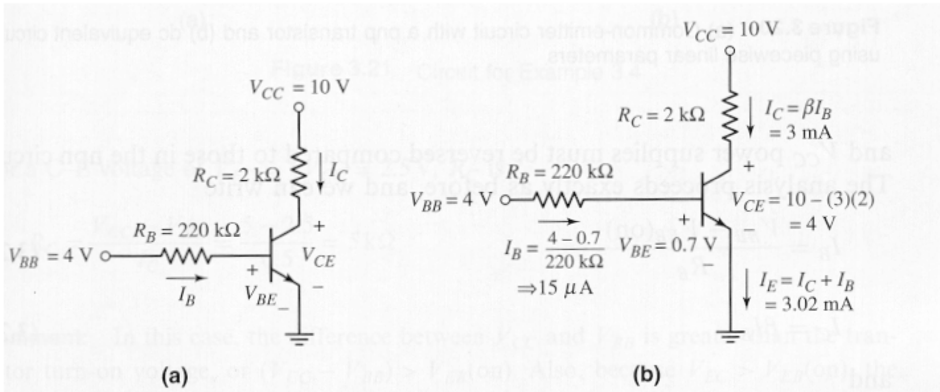


Figure 3.19 Circuit for Example 3.3

Note: Since V_{CE} came out to be 4 V (> $(V_{CE})_{sat}$ = 0.1 V), the BJT is indeed Forward-Active as initially assumed!

Load Line Analysis of Figure 3.19.

KVL Around Base Loop: $V_{BB} = I_B R_B + V_{BE} \Rightarrow I_B = -V_{BE}/R_B + V_{BB}/R_B$

KVL Around Collector Loop: $Vcc = I_C R_C + V_{CE} \Rightarrow I_C = -V_{CE}/R_C + Vcc/R_C$

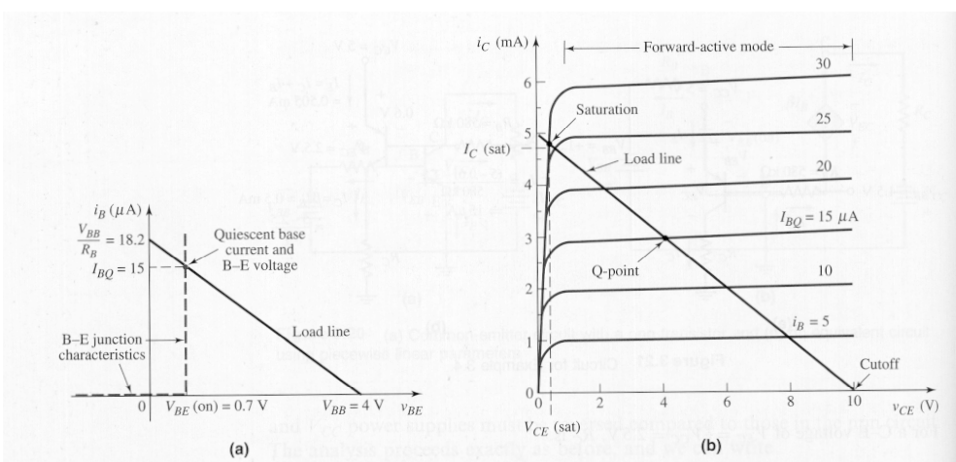


Figure 3.22 (a) Base–emitter junction characteristics and the input load line and (b) common-emitter transistor characteristics and the collector–emitter load line

DC Equivalent Forward-Active Model of PNP BJT

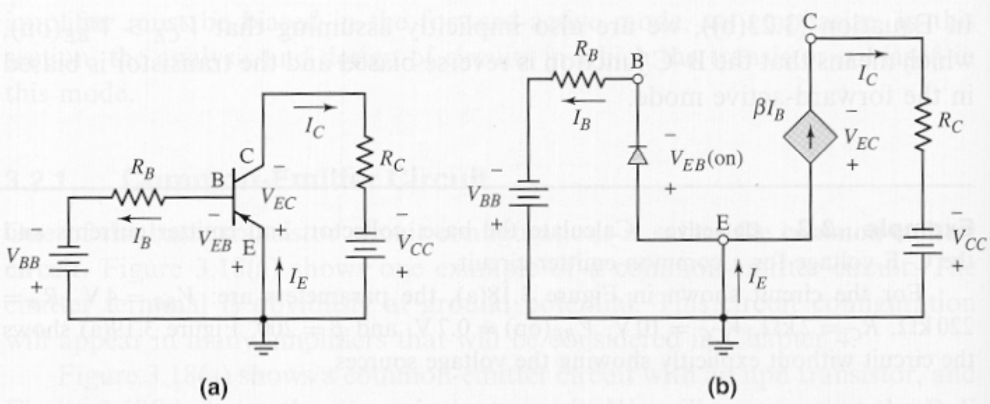
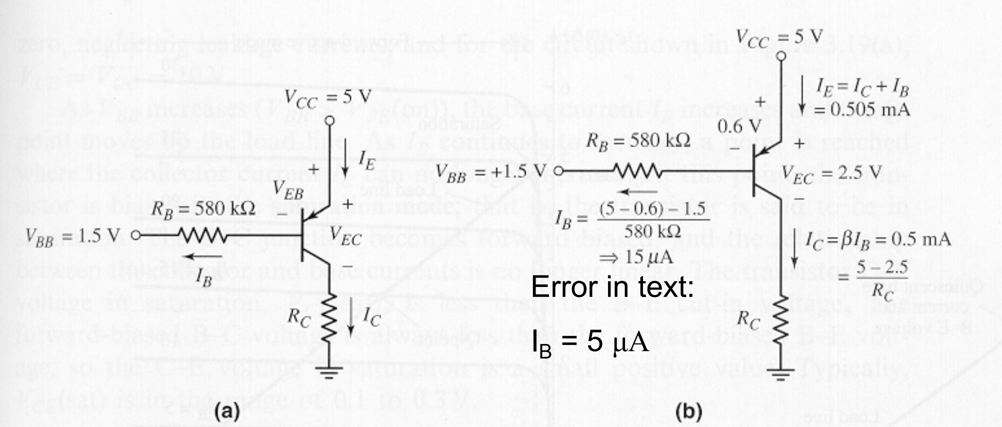


Figure 3.20 (a) Common-emitter circuit with a pnp transistor and (b) dc equivalent circuit using piecewise linear parameters

PNP BJT DC Analysis

($\beta_F = 100$, V_{EBON} = 0.6 V, V_{ECSAT} = 0.2V) **FIND: Rc so Vec = Vcc/2**

Since $V_{EC} > V_{ECSAT}$, NPN BJT is Forward Active.



Error in text:

I_B = 5 μA

Figure 3.21 Circuit for Example 3.4

Final Result: Rc = (Vcc – Vec)/Ic = (5-2.5)/0.5mA = 5 kohms.

NPN BJT Analysis Example when BJT Saturated

(β_F = 100, V_{BEON} = 0.7 V, V_{CESAT} = 0.2V)

Initially assume forward-active, but when we discover that this assumption leads to VCE = -3.28 V < V_{CESAT}, we must assume BJT is saturated.

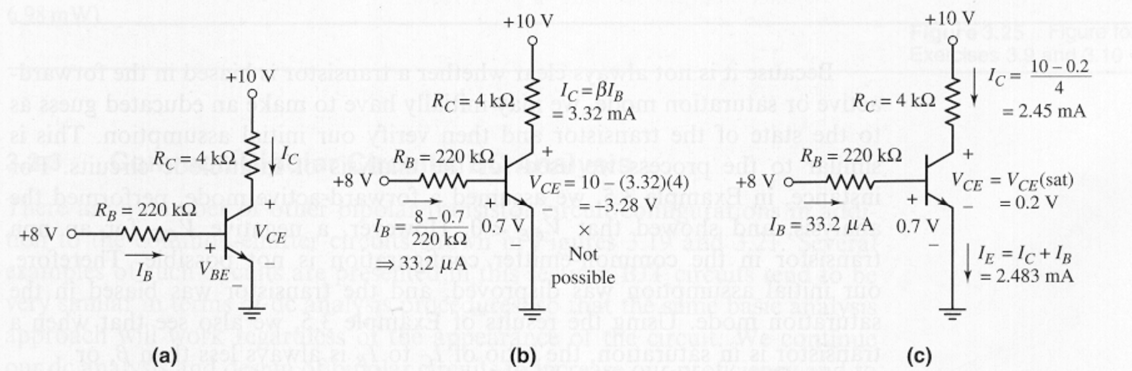


Figure 3.23 Circuit for Example 3.5

Problem-Solving Technique: Bipolar DC Analysis

Analyzing the dc response of a bipolar transistor circuit requires knowing the mode of operation of the transistor. In some cases, the mode of operation may not be obvious, which means that we have to guess the state of the transistor, then analyze the circuit to determine if we have a solution consistent with our initial guess. To do this, we can:

1. Assume that the transistor is biased in the forward-active mode in which case $V_{BE} = V_{BE}(\text{on})$, $I_B > 0$, and $I_C = \beta I_B$.
2. Analyze the "linear" circuit with this assumption.
3. Evaluate the resulting state of the transistor. If the initial assumed parameter values and $V_{CE} > V_{CE}(\text{sat})$ are true, then the initial assumption is correct. However, if $I_B < 0$, then the transistor is probably cut off, and if $V_{CE} < 0$, the transistor is likely biased in saturation.
4. If the initial assumption is proven incorrect, then a new assumption must be made and the new "linear" circuit must be analyzed. Step 3 must then be repeated.

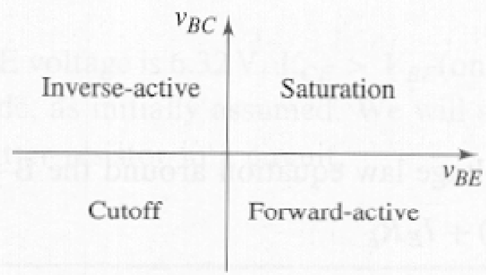


Figure 3.24 Bias conditions for the four modes of operation of an npn transistor

Example 3.6 **Objective:** Calculate the characteristics of a circuit containing an emitter resistor.

For the circuit shown in Figure 3.26(a), let $V_{BE}(\text{on}) = 0.7\text{ V}$ and $\beta = 75$.

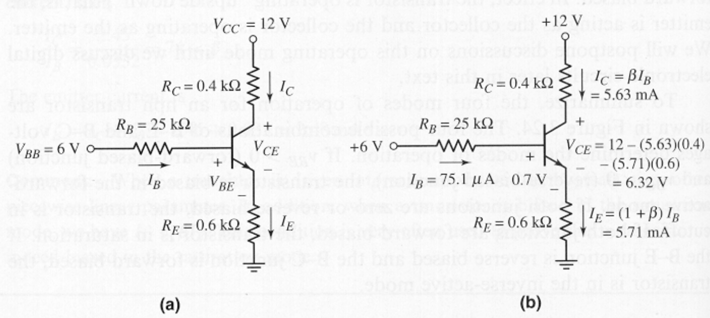


Figure 3.26 Circuit for Example 3.6

Solution:

***Q*-Point Values:**

Writing the Kirchhoff's voltage law equation around the B–E loop, we have

$$V_{BB} = I_B R_B + V_{BE}(\text{on}) + I_E R_E \qquad (3.29)$$

Assuming the transistor is biased in the forward-active mode, we can write $I_E = (1+\beta)I_B$. We can then solve Equation (3.29) for the base current:

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B + (1+\beta)R_E} = \frac{6 - 0.7}{25 + (76)(0.6)} \Rightarrow 75.1\ \mu\text{A}$$

Plot Load Line using KVL:

$$V_{CC}=R_CI_C+V_{CE}+(\beta_F+1)(I_C/\beta_F)R_E$$

$$=> \quad I_c = -V_{CE}/(R_c+R_E(\beta_F+1)/\beta_F) + V_{cc}/(R_c+R_E(\beta_F+1)/\beta_F)$$

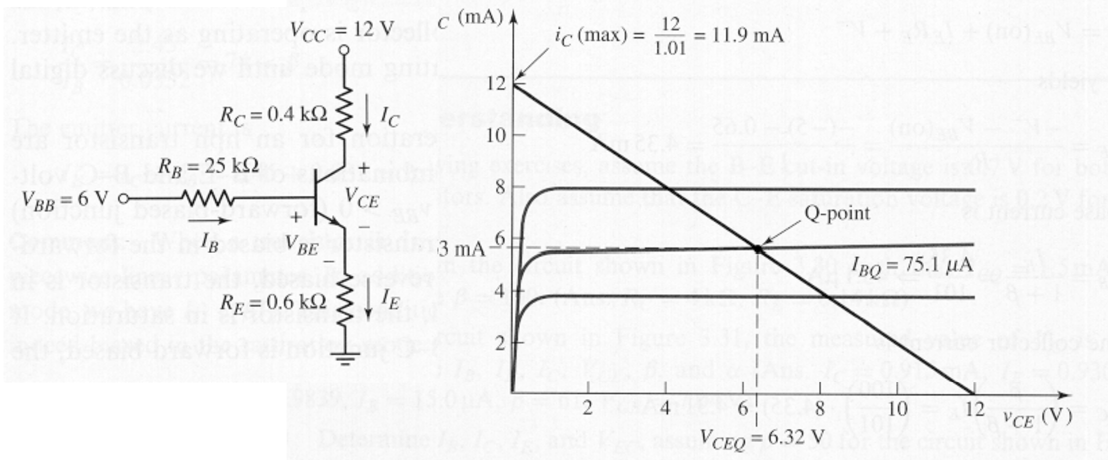


Figure 3.27 Load line for the circuit in Figure 3.26

Example 3.7 **Objective:** Calculate the characteristics of a circuit containing both a positive and a negative power supply voltage.

For the circuit shown in Figure 3.28, let $V_{BE}(\text{on}) = 0.65$ V and $\beta = 100$. Even though the base is at ground potential, the B–E junction is forward biased through R_E and V^-.

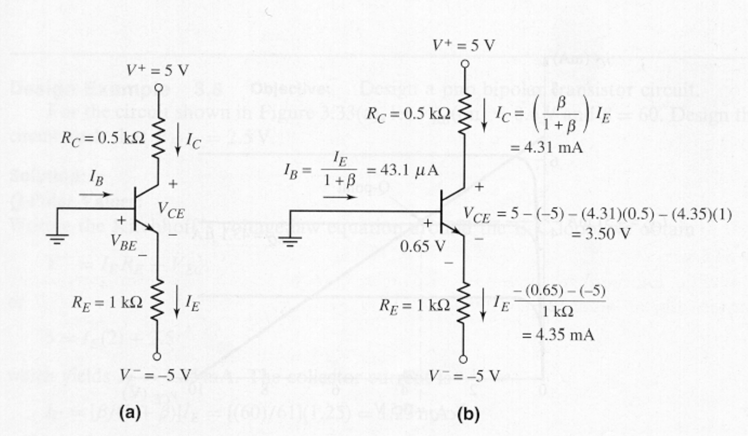


Figure 3.28 Circuit for Example 3.7

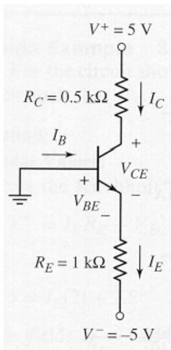
Solution:
Load Line:
The load line equation is

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right] = (5-(-5)) - I_C\left[0.5 + \left(\frac{101}{100}\right)(1)\right]$$

or

$$V_{CE} = 10 - I_C(1.51)$$

The load line and the calculated Q-point are shown in Figure 3.29.



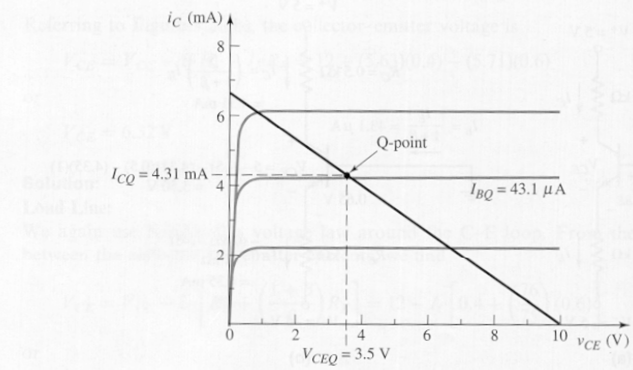


Figure 3.29 Load line for the circuit in Figure 3.28

Example 3.9 **Objective:** Calculate the characteristics of an npn bipolar circu with a load resistance. The load resistance can represent a second transistor stage cor nected to the output of a transistor circuit.

For the circuit shown in Figure 3.36(a), the transistor parameters are: $V_{BE}(\text{on})$ 0.7 V, and $\beta = 100$.

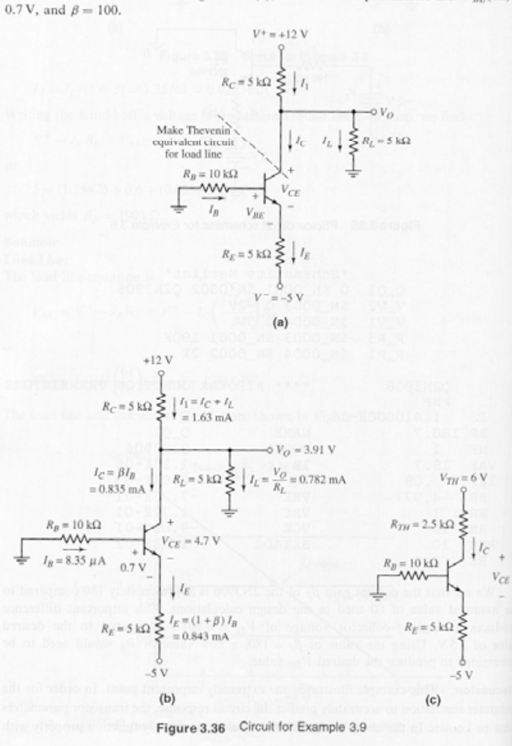


Figure 3.36 Circuit for Example 3.9

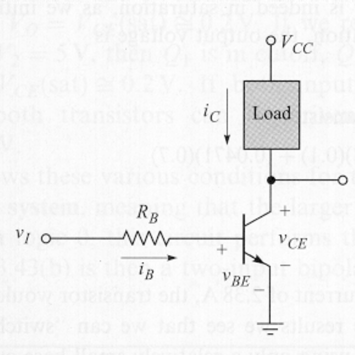


Figure 3.42 An npn bipolar inverter circuit used as a switch

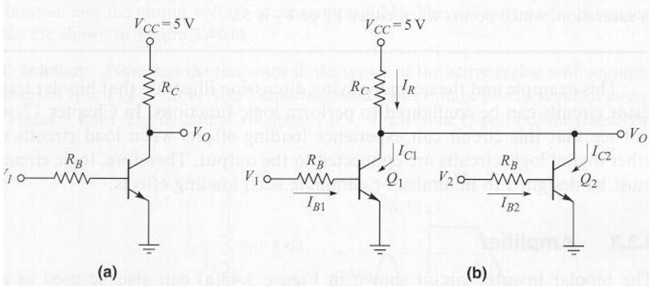


Figure 3.43 A bipolar (a) inverter circuit and (b) NOR logic gate

Table 3.2 The bipolar NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	5
5	0	0.2
0	5	0.2
5	5	0.2

Solution: The following table indicates the equations and results for this example.

Condition	V_O	I_R	Q_1	Q_2
$V_1 = 0$, $V_2 = 0$	5 V	0	$I_{B1} = I_{C1} = 0$	$I_{B2} = I_{C2} = 0$
$V_1 = 5$ V, $V_2 = 0$	0.2 V	$\frac{5-0.2}{1} = 4.48$ mA	$I_{B1} = \frac{5-0.7}{20} = 0.215$ mA, $I_{C1} = I_R = 4.8$ mA	$I_{B2} = I_{C2} = 0$
$V_1 = 0$, $V_2 = 5$ V	0.2 V	4.8 mA	$I_{B1} = I_{C1} = 0$	$I_{B2} = 0.215$ mA, $I_{C2} = I_R = 4.8$ mA
$V_1 = 5$ V, $V_2 = 5$ V	0.2 V	4.8 mA	$I_{B1} = 0.215$ mA, $I_{C1} = \frac{I_R}{2} = 2.4$ mA	$I_{B2} = 0.215$ mA, $I_{C2} = \frac{I_R}{2} = 2.4$ mA

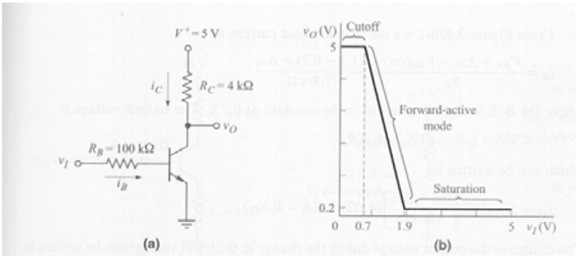


Figure 3.44 (a) A bipolar inverter used as an amplifier; (b) the inverter voltage transfer characteristics

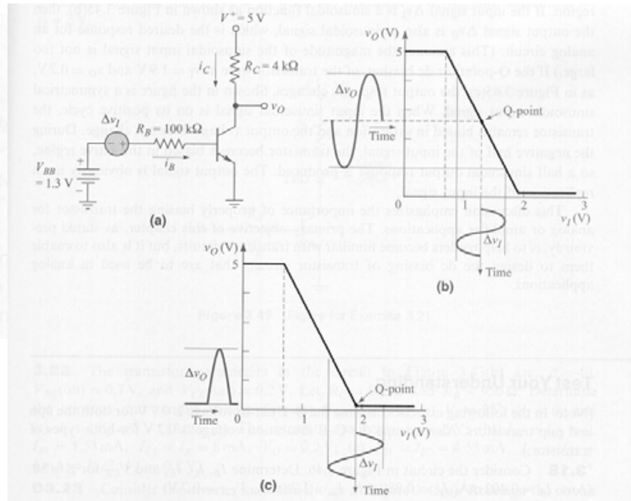


Figure 3.45 (a) The inverter circuit with both a dc and an ac input signal; (b) the dc voltage transfer characteristics, *Q*-point, and sinusoidal input and output signals; (c) the transfer characteristics showing improper dc biasing

Single Base Bias Resistor Circuit

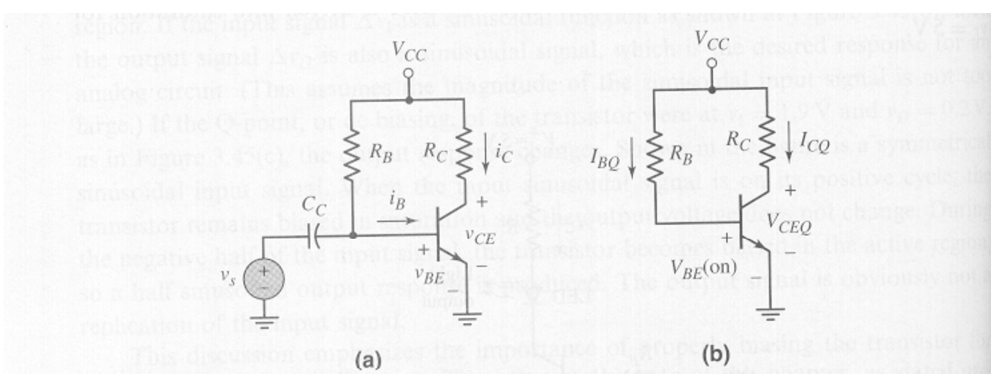


Figure 3.50 (a) Common-emitter circuit with a single bias resistor in the base and (b) dc equivalent circuit

Design Example 3.13 **Objective:** Design the circuit shown in Figure 3.50(to yield a given I_{CQ} and V_{CEQ}.

Assume that $V_{CC} = 12\,\text{V}$, $\beta = 100$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$. The Q-point values a be $I_{CQ} = 1\,\text{mA}$ and $V_{CEQ} = 6\,\text{V}$.

Solution: The collector resistance can be found from

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{12 - 6}{1} = 6\,\text{k}\Omega$$

The base current must then be

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1\,\text{mA}}{100} \Rightarrow 10\,\mu\text{A}$$

and the base resistance is determined to be

$$R_B = \frac{V_{CC} - V_{BE}(\text{on})}{I_{BQ}} = \frac{12 - 0.7}{10\,\mu\text{A}} = 1.13\,\text{M}\Omega$$

Load Line:

KVL: Vcc = IcRc+Vce

=> Ic = -Vce/Rc + Vcc/Rc

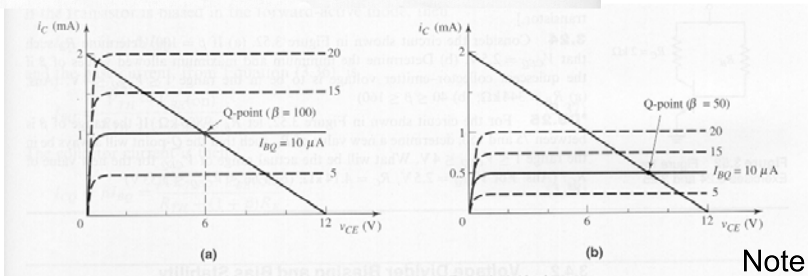


Figure 3.51 Transistor characteristics and load line for the circuit in Example 3.13 when (a) $\beta = 100$ and (b) $\beta = 50$

Note the **<u>LARGE</u>**

<u>VARIATION</u> in I_{CQ} and V_{CEQ} as β is halved!

3-Resistor “Voltage Divider” DC Bias Network

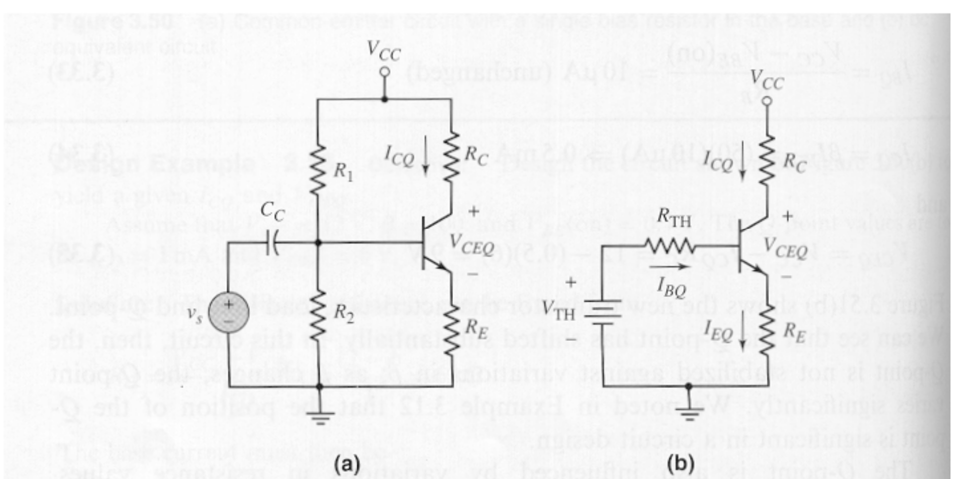


Figure 3.53 (a) A common-emitter circuit with an emitter resistor and voltage divider bias circuit in the base; (b) the dc circuit with a Thevenin equivalent base circuit

Analysis of 3-Resistor Bias Network

Vth = R2/(R1+R2)Vcc

Rth = R1 // R2 = R1*R2/(R1 + R2)

KVL around base loop:

$$Vth = I_{BQ}*R_{TH}+V_{BEon} + (1 + \beta)I_{BQ}*R_E$$

$$\Rightarrow I_{BQ} = (V_{TH} - V_{BEON})/\{R_{TH} + (1 + \beta)R_E\}$$

$$I_{CQ} = \beta I_{BQ} = \beta(V_{TH} - V_{BEON})/\{R_{TH} + (1 + \beta)R_E\}$$

Design for "Bias Stability" w.r.t. β

Problem: β varies over a wide range. For the 2N2222, 80 < β < 300). How do we keep the dc bias current and voltage from changing as β changes?

Solution: For the 3-resistor bias network, we found on the previous slide

$$I_{CQ} = \beta(V_{TH} - V_{BEon})/\{R_{TH} + (1+ \beta)R_E\}$$

If we make $R_{TH} << (1+ \beta)R_E$ then

$$I_{CQ} \approx \beta(V_{TH} - V_{BEon})/(1+ \beta)R_E$$

Since **β /(1+ β) ≈ 1 (since β is typically > 100)**

$$I_{CQ} \approx (V_{TH} - V_{BEon})/R_E$$

Thus we can make I_{CQ} approximately *independent* of β variation, simply by choosing component values so that

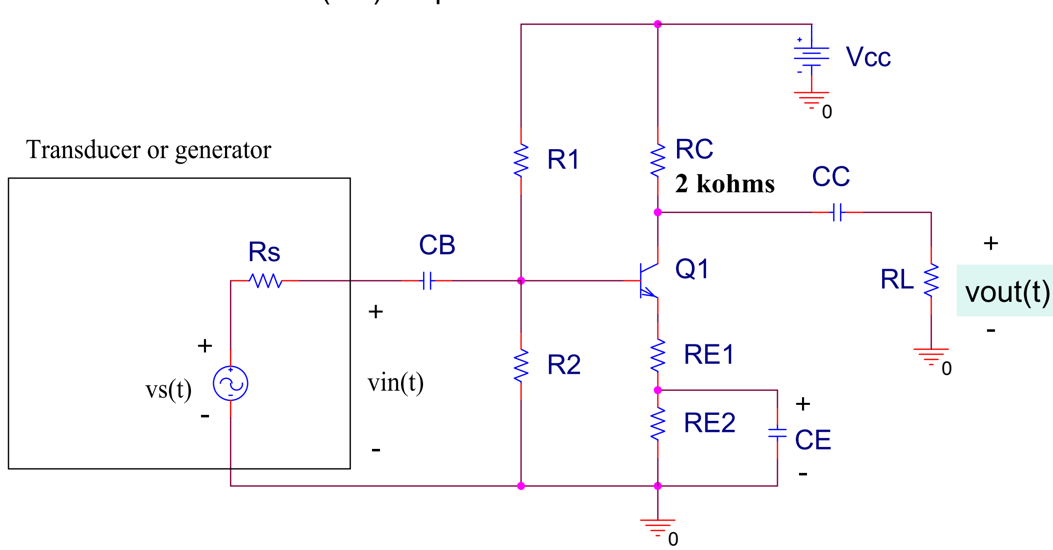
$$(1+ \beta)R_E = 10R_{TH}$$

BJT Common-Emitter (CE) Audio Amplifier Analysis and Design

We will start with the complete circuit of a CE amplifier, then we will proceed to its DC model to find its Q-point (Icq, Vceq), then its AC model to find its input resistance, output resistance, and its small-signal gain

Av = vout(t) / vin(t)

BJT Common-Emitter (CE) Amplifier



This is the complete CE amplifier circuit that we will analyze using the principle of Linear Superposition. First we shall find the dc bias (quiescent) portion of Ib, Vce, etc. due to the dc source (Vcc) acting alone, with vs(t) set to 0. Then we will find the ac portion of the response due to vs(t) acting alone with Vcc set to 0.

DC Bias Point Design Problem

In a design problem, you are given the desired Q-point, and you must choose the component values needed to "make this Q-point happen"

We shall follow two "design rules of thumb" to promote bias stability:

1. Choose component values so that $(\beta + 1)R_E >> R_{TH}$, Let us make

$$(\beta + 1)R_E = 10R_{TH}$$

2. V_E should be the same order of magnitude as Vbe(on), so we let us make

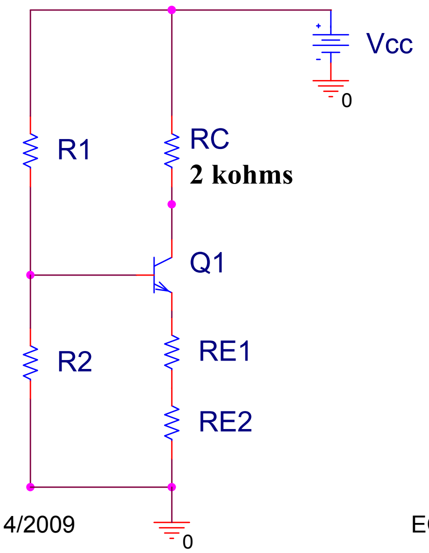
$$V_E = 1.0 \text{ V.}$$

DC Bias Point Design Example

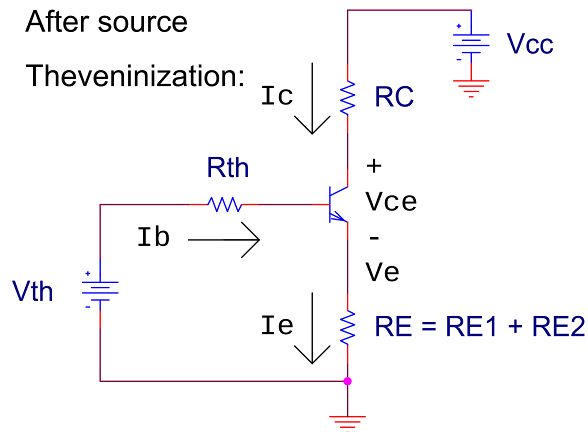
Given: RC = 2 kilohms, β = 100, Vbe(on) = 0.7 V

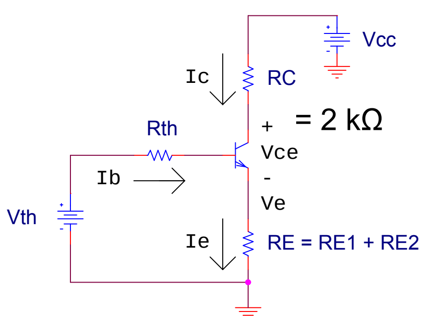
Find: R1, R2, RE = RE1+RE2, and Vcc such that BJT is biased at the following Q-Point: (Vceq = 2 V, Icq = 1 mA)

Begin by constructing the dc model of the circuit. Set vs(t) = 0, replace all capacitors by open circuits. The dc model becomes:



After source Theveninization:





We require that Ic = Icq = 1 mA

Vce = Vceq = 2 V

also that V_E = 1.0 V (rule of thumb)

Thus Vcc = Ic*Rc + Vceq + Ve

= 1 mA * 2 kΩ + 2 + 1

= 5 V

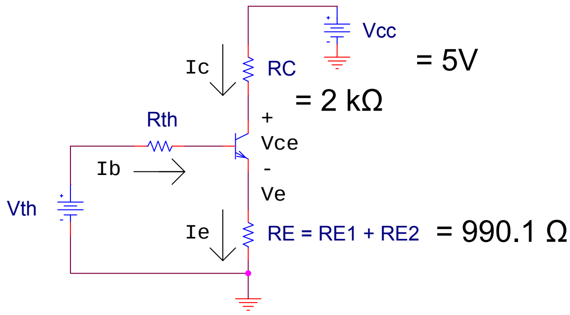
Note: Vth = (5 V)(R2/(R1+R2))

Rth = R1 // R2

But we cannot evaluate Vth or Rth, since we do not know the values of R1 and R2 yet!

We may now calculate RE:

RE = VE/IE = 1 V / (Ic(β+1)/β) = 1 V / (1 mA*(101/100)) = <u>990.1 Ω</u>



Note: Vth = (5 V)(R2/(R1+R2))

Rth = R1 // R2

KVL around the base loop =>

Vth = Ib*Rth + 0.7 V + (β+1)*Ib*RE => Ib = (Vth – 0.7 V)/(Rth + (β+1)RE)

Ic = Icq = β*Ib = β(Vth – 0.7 V)/(Rth + (β+1)RE) = 1 mA (desired Icq)

Also, because of Design Rule of Thumb #1, we require

Rth = 0.1*(β+1)RE = 0.1*(101)*990.1 Ω = 10.0 kΩ

Substituting this value of Rth into the equation for Icq:

β(Vth – 0.7 V)/(Rth + (β+1)RE) = Icq

100(Vth – 0.7 V)/(10.0 kΩ + (101)(990.1 Ω) = 1.0 mA

=> <u>Vth = 1.80 V</u>

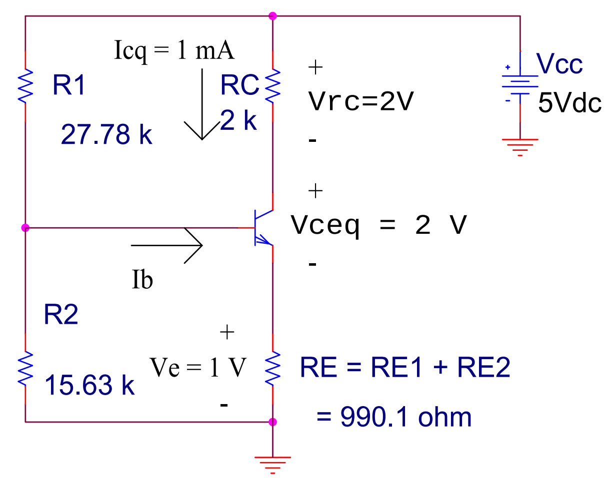
From the equations for Rth and Vth, we may solve for R1 and R2

Rth = R1*R2/(R1+R2) = 10 kΩ and Vth = Vcc*R2/(R1+R2) = 1.80 V

=> <u>R1 = 27.77 kΩ</u> and <u>R2 = 15.625 kΩ</u>

Final dc bias network design for β = 100;

Q-Point: (Icq = 1 mA, Vceq = 2 V)



DC Bias Point <u>Analysis</u> Example Problem

In an analysis problem, all of the component values are given, and you are to find the resulting Q-point

DC Bias Point *Analysis* Example:

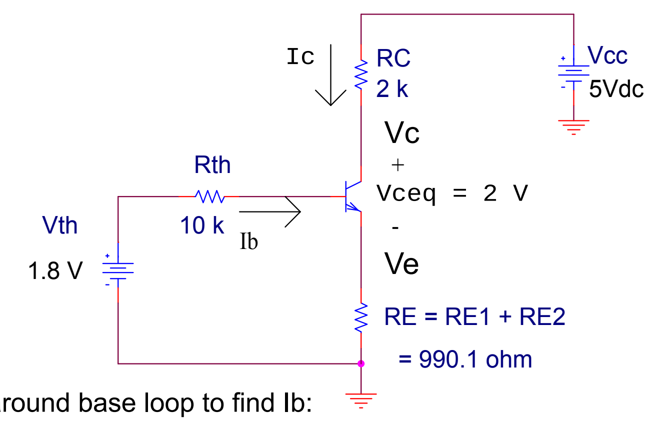
Given: The dc bias circuit designed above.

Find: the new Q-point if β is increased from 100 to 200. (Hopefully it will not change much, since we specifically designed the circuit to have its Q-point stable w.r.t. changes in β.)

Note: Since we have changed β and kept everything else the same, we can no longer assume the "rules of thumb" hold. That is, VE no longer = 1 V, nor does Rth = $0.1(\beta+1)R_E$.

Solution: Begin by Theveninizing source

Vth = Vcc(R2/(R2+R1)) = 1.8 V and Rth = R1 // R2 = 10 kΩ



Write KVL around base loop to find Ib:

Vth = Ib*Rth + 0.7 V + Ib(β+1)RE

⇒ Ib = (Vth – 0.7V)/(Rth + (β+1)RE) = 5.263 μA => Ic = β*Ib = <u>1.053 mA</u>

Vc = Vcc – β*Ib*RC = 5 – 200(5.263 μA)(2 kΩ)= 2.895 V

Ve = (β+1)Ib*RE = 201(5.263 μA)(990.1 Ω) = 1.047 V

Thus Vce = Vc – Ve = 2.895 – 1.047 = <u>1.847 V</u>.

Thus the Q-point corresponding to β = 200 (**<u>Icq = 1.053 mA, Vceq = 1.847 V</u>**)

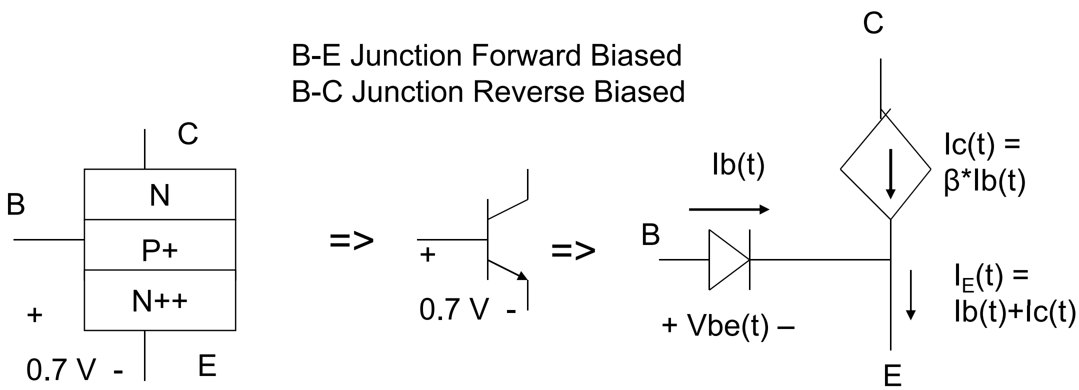
is relatively close to original Q-point corresponding to β = 100 (**<u>Icq = 1 mA, Vceq = 2 V</u>**)

AC Model of Forward-Active NPN BJT

In this section, we shall derive a "linearized" ac small-signal model of the BJT that is analogous to the "rd" linearized ac small-signal model of the diode that was derived earlier.

For a forward-active BJT, we know that the

B-E Junction Forward Biased
B-C Junction Reverse Biased



For forward-biased diode junction,

Ib = Is(exp[Vbe/(ηV_T)] – 1)

Ib = Is*exp[Vbe/(ηV_T)] (fwd-bias approx)

(Note: $\eta \approx 1$ for IC BJT, $\eta \approx 2$ for Discrete BJT)

The total base current and base-emitter voltage can be divided into a relatively large dc (quiescent) bias value and a relatively small ac signal

Ib(t) = Ibq + ib(t) Vbe(t) = Vbq + vbe(t)

$Ib(t) = Ibq + ib(t)$ $Vbe(t) = Vbq + vbe(t)$

$= Ibq + \Delta Ib$ $= Vbq + \Delta Vbe$

$$Ib(t) = Is*\exp(Vbe(t)/ (\eta V_T)$$

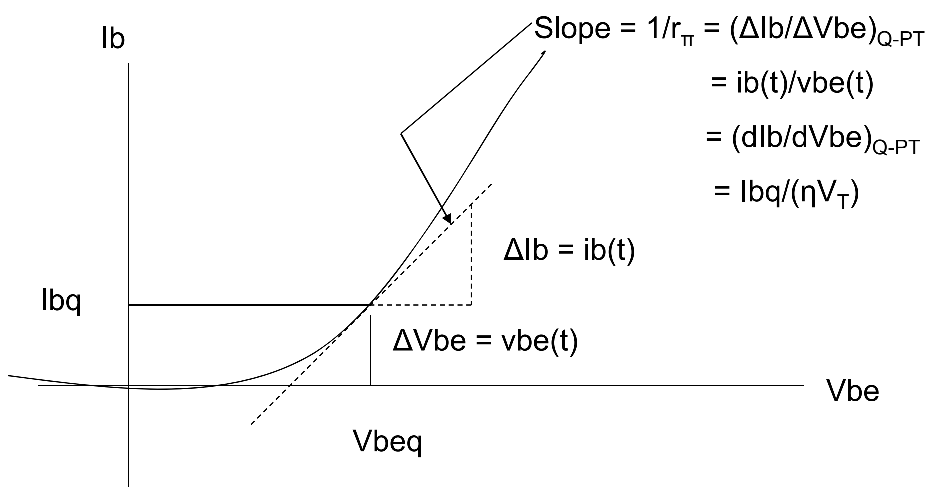
Working as we did with the ac model of the diode, let us define r_π as the ratio vbe(t)/ib(t). Then the base-emitter diode junction of the BJT can be thought of as a (linear) resistor of value "r_π" that converts the ac component of base current ib(t) into the ac component of base-emitter voltage vbe(t) via the equation "$vbe(t) = ib(t)*r_\pi$".

Let us determine an expression for r_π

$$1/r_\pi = ib(t)/vbe(t) = (\Delta Ib/\Delta Vbe)_{Q\text{-}PT} = (dIb/dVbe)_{Ibq,Vbeq}$$

$$= (1/(\eta V_T)^* Is*\exp(Vbe(t)/ (\eta V_T))_{Q\text{-}PT}$$

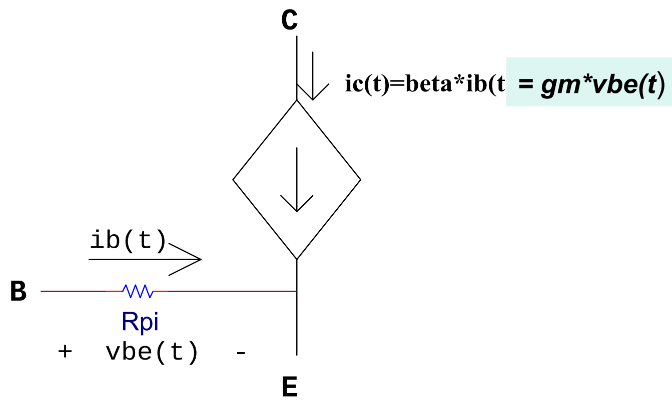
$$= (1/(\eta V_T))*Ib)_{Q\text{-}PT} = Ibq/(\eta V_T)$$



r_π is used in place of the B-E junction diode in the small-signal AC model of the BJT in order to change the ac portion of base current ib(t) into the ac portion of base-emitter voltage vbe(t)

$$vbe(t) = r_\pi*ib(t)$$

AC Model of NPN BJT



Note: ic(t) = βib(t) = β*(vbe(t)/r_π) = (β/ r_π)vbe(t) = gm*vbe(t)

Where gm is the BJT's transconductance = (β/ r_π)

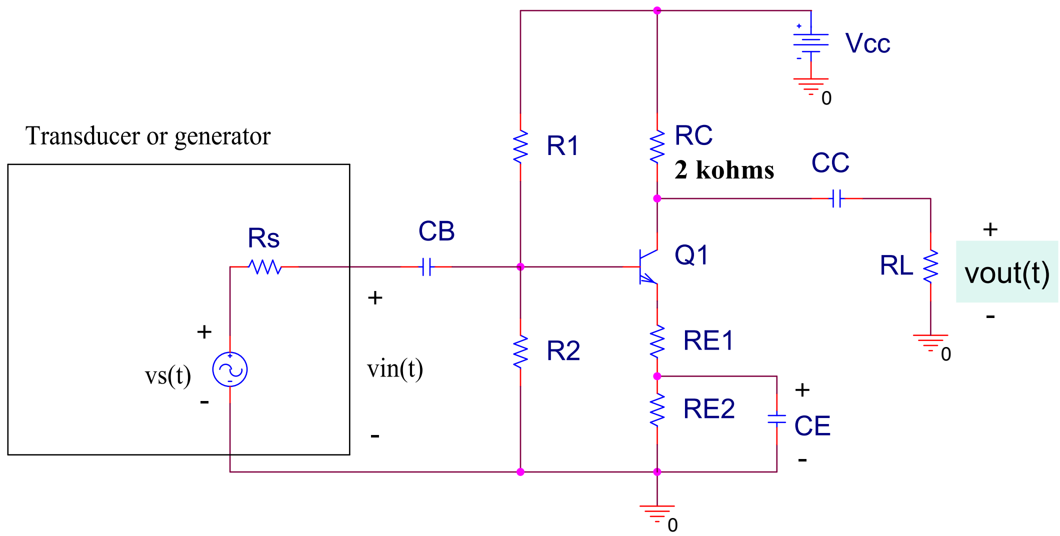
Note gm = ic/vbe has units of A/V = mhos or Siemens,

And β = ic/ib which makes it a <u>unitless</u> quantity.

AC Model of BJT Amplifier

In this section, we shall construct the ac model of the CE amplifier circuit, and from it, we shall derive the small-signal ac voltage gain, input impedance, output impedance, etc.

BJT Common-Emitter (CE) Amplifier

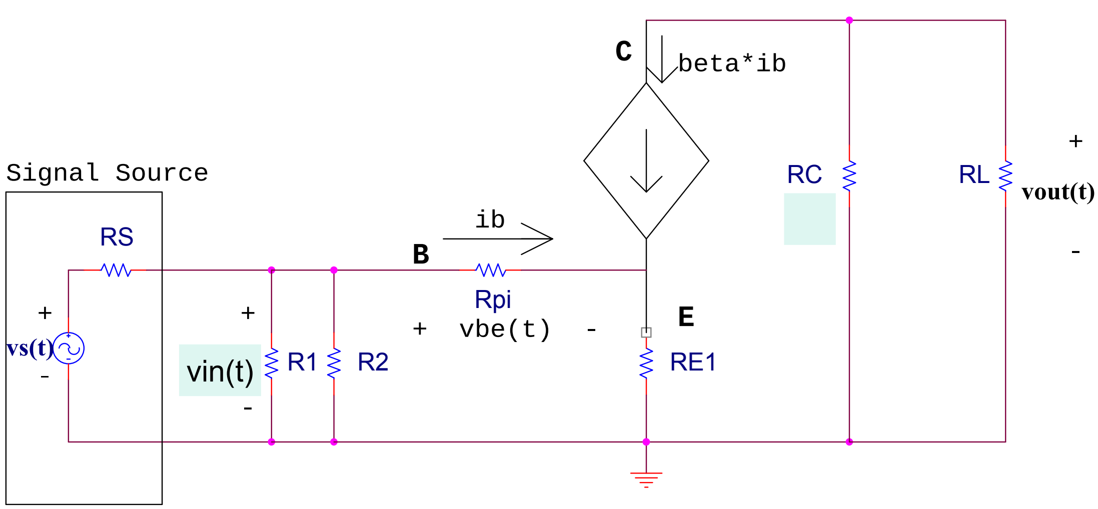


This is the complete CE amplifier circuit that we will analyze using the principle of Linear Superposition. First we shall find the dc bias (quiescent) portion of Ib, Vce, etc. due to the dc source (Vcc) acting alone, with vs(t) set to 0. Then we will find the ac portion of the response due to vs(t) acting alone with Vcc set to 0.

AC Model of CE Amplifier Circuit

Set Vcc = 0, replace all capacitors by short circuits.

*(We assume that all capacitors are sufficiently high in value so that the magnitude of the impedance of each capacitor (1/(2*Pi*f*C)) is << than the surrounding resistor values.)*



AC Transducer Voltage Gain Calculations

Define the Transducer Voltage Gain **Av_T = vout / vin**

First find ib by writing a KVL equation around the base loop:

$$vin = ib \cdot r\pi + (\beta \cdot ib + ib) \cdot RE1$$

=> $$ib = \frac{vin}{[r\pi + RE1 \cdot (\beta + 1)]}$$

Now find vout(t) by writing a KVL equation around the collector loop

$$vout = -\beta \cdot ib \cdot \frac{(RC \cdot RL)}{RC + RL}$$

$$vout = -\beta \cdot \frac{vin}{[r\pi + (\beta + 1) \cdot RE1]} \cdot \frac{RC \cdot RL}{(RC + RL)}$$

$$Av_T = \frac{vout}{vin} = \frac{-\beta}{r\pi + (\beta + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)}$$

General Equation for transducer voltage gain:

$$Av_T = \frac{vout}{vin} = \frac{-\beta}{r\pi + (\beta + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)}$$

Special Case 1: If RE is fully bypassed (CE is connected across entire emitter resistor, so RE1 = 0), the equation for A_{VT} reduces to:

$$Av_T = \frac{-\beta}{r\pi} \cdot \frac{RC \cdot RL}{(RC + RL)}$$

This results in the highest possible voltage gain, but the gain is very dependent upon β, and thus the gain cannot be tightly controlled from one circuit board to the next, since β varies from one BJT to another, even if they are of the same type.

Special Case 2: If $(\beta+1)RE1 \gg r_\pi$, the general equation for A_{VT} reduces to:

$$A_{VT} = \frac{-\beta}{(\beta + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)}$$

For β sufficiently large, β/(β+1) ≈ 1, so

$$A_{VT} = \frac{-1}{RE1} \cdot \frac{RC \cdot RL}{RC + RL}$$

Note in this case, Av_T is **independent of β**, and is set solely by the resistor ratio -(RC // RL) / RE1. Unfortunately, this usually results in a relatively small A_{VT}.

In our design example, let RL = 4 kΩ

Given:

$\eta := 2$ (This is a discrete BJT) $\beta low := 100$ $\beta high := 200$

$R1 := 27.78 \cdot k\Omega$ $R2 := 15.63 \cdot k\Omega$ $RC := 2 \cdot k\Omega$ $RL := 4 \cdot k\Omega$

Find AC model B-E resistance "rπ" for β=100 and for β = 200 :

$$r_{\pi 100} := \frac{\eta \cdot 26 \cdot mV}{\left(\frac{1.0 \cdot mA}{\beta low}\right)} \qquad r_{\pi 100} = 5.2 \times 10^{3} \Omega$$

$$r_{\pi 200} := \frac{\eta \cdot 26 \cdot mV}{\left(\frac{1.053 \cdot mA}{\beta high}\right)} \qquad r_{\pi 200} = 9.877 \times 10^{3} \Omega$$

Case 1: Fully Bypassed Case (CE across entire RE)

=> $RE2 := 990.1 \cdot \Omega$ $RE1 := 0 \cdot \Omega$

$$A_{vT200} := \frac{-\beta high}{r_{\pi 200} + (\beta high + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)} \qquad A_{vT200} = -27$$

$$A_{vT100} := \frac{-\beta low}{r_{\pi 100} + (\beta low + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)} \qquad A_{vT100} = -25.641$$

Case 2: Partially Bypassed Case (CE across all but 50 ohms of RE)

=> $RE2 := 940.1 \cdot \Omega$ $RE1 := 50 \cdot \Omega$

$$A_{vT200} := \frac{-\beta high}{r_{\pi 200} + (\beta high + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)} \qquad A_{vT200} = -13.382$$

$$A_{vT100} := \frac{-\beta low}{r_{\pi 100} + (\beta low + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)} \qquad A_{vT100} = -13.008$$

Case 3: Unbypassed Case (CE not present)

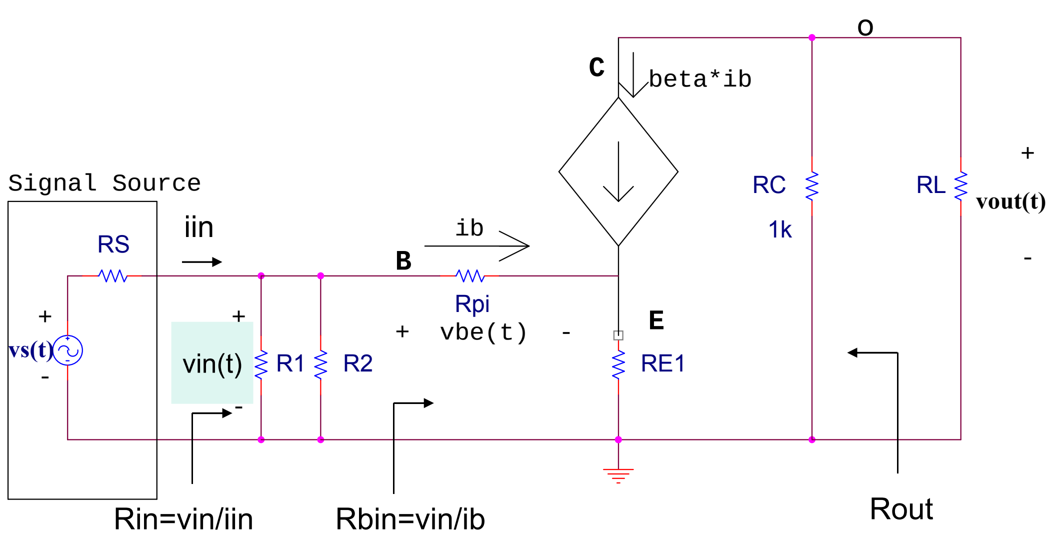
=> $RE2 := 0 \cdot \Omega$ $RE1 := 990.1 \cdot \Omega$

$$A_{vT200} := \frac{-\beta high}{r_{\pi 200} + (\beta high + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)} \qquad A_{vT200} = -1.277$$

$$A_{vT100} := \frac{-\beta low}{r_{\pi 100} + (\beta low + 1) \cdot RE1} \cdot \frac{RC \cdot RL}{(RC + RL)} \qquad A_{vT100} = -1.267$$

Input Impedance Rin

Input Impedance (Rin) is the impedance seen looking into the input terminals, Rin is the ratio of the input current to the input voltage (iin/vin)



KVL base loop => vin = ib*r_π + (β+1)*ib*RE1

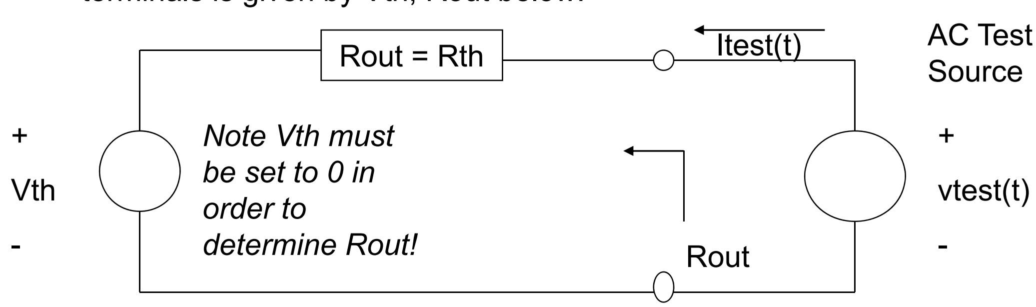
⇒ Rbin = vin/ib = r_π + (β+1)*RE1

Rin = vin/iin = Rbin // R1 // R2

Output Impedance Rout

Rout is the Thevenin Equivalent resistance seen looking into the output terminals

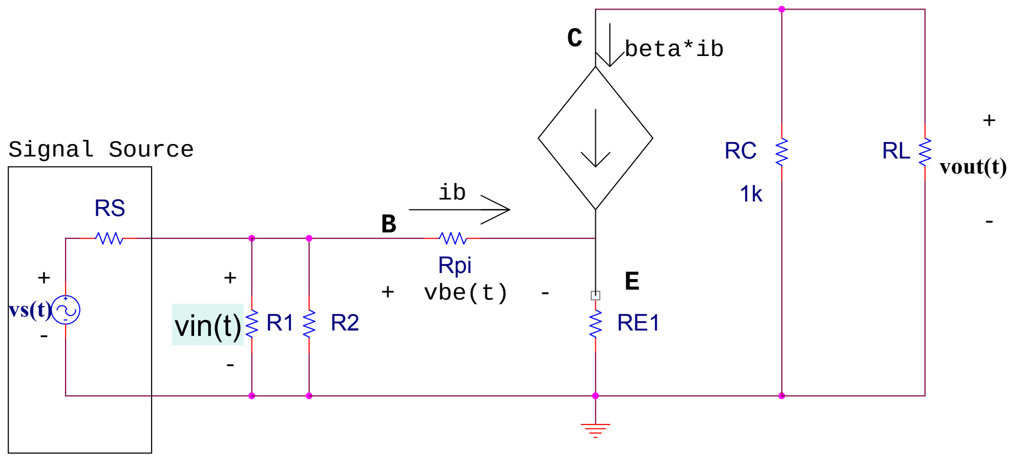
Imagine that the Thevenin Equivalent looking into the output terminals is given by Vth, Rout below:



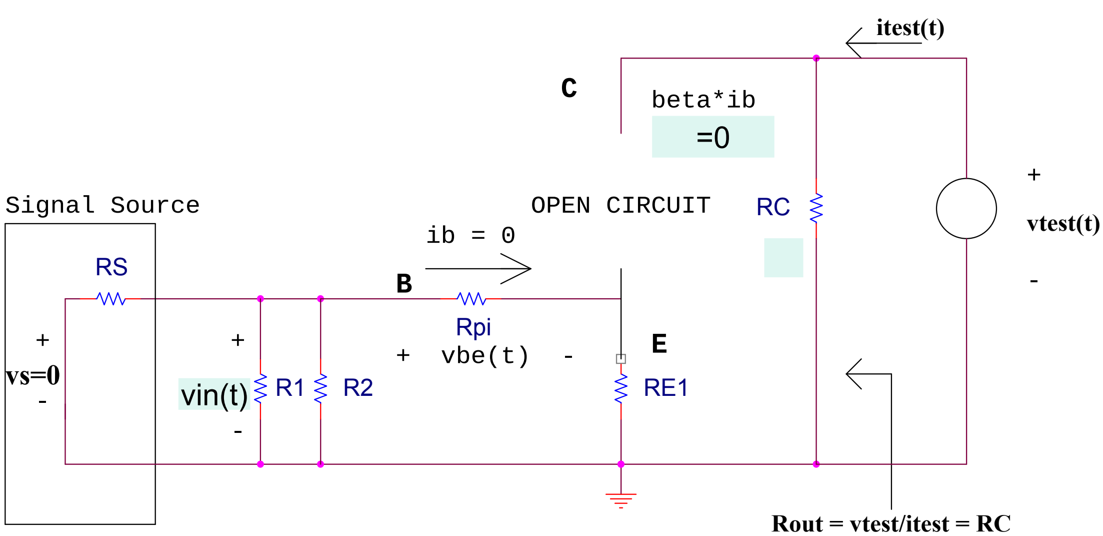
Rout can be determined by connecting an ac small-signal test source, vtest(t) across the output terminals ***AND BY SETTING Vth = 0***. Then

$$\textbf{Rout} = \{vtest(t)/itest(t)\}_{Vth = 0}$$

Vth represents the effects of all independent sources in the circuit. Therefore, you must set all sources in the actual circuit = 0. In this case, you must set vs(t) = 0.

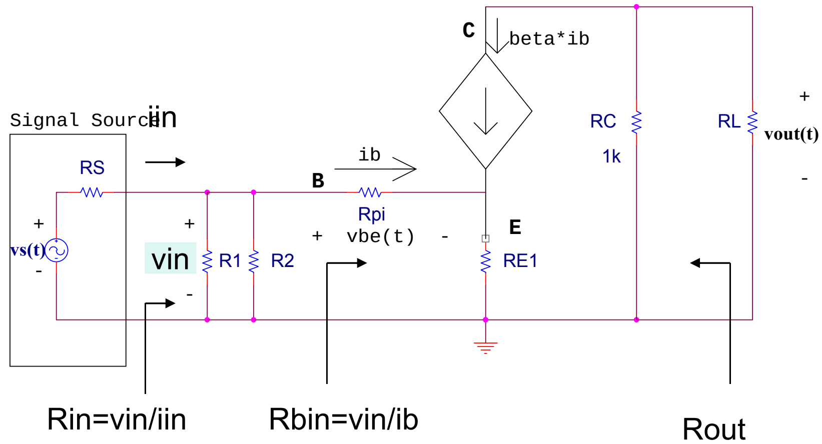


If vs(t) is set to 0 in this circuit, ib will = 0, and so ic = βib = 0, thus the controlled current source may be erased in the diagram above, resulting in….



It should be apparent, by inspection, that

Rout = vtest/itest = RC



For Complete Bypass Example (Case 1, RE1 = 0, β = 100)

$$\text{Rbin} := r_{\pi 100} \qquad \text{Rbin} = 5.2 \times 10^{3}\,\Omega$$

$$\text{Rin} := \frac{1}{\frac{1}{\text{Rbin}} + \frac{1}{\text{R1}} + \frac{1}{\text{R2}}} \qquad \text{Rin} = 3.421 \times 10^{3}\,\Omega$$

$$\text{Rout} := \text{RC} \qquad \text{Rout} = 2 \times 10^{3}\,\Omega$$

For Partial Bypass Example (Case 2, RE1 = 50Ω, β = 100)

$$\text{Rbin} := r_{\pi 100} + (\beta\text{low} + 1)\cdot 50\cdot\Omega \qquad \text{Rbin} = 1.025 \times 10^{4}\,\Omega$$

$$\text{Rin} := \frac{1}{\frac{1}{\text{Rbin}} + \frac{1}{\text{R1}} + \frac{1}{\text{R2}}} \qquad \text{Rin} = 5.062 \times 10^{3}\,\Omega$$

$$\text{Rout} := \text{RC} \qquad \text{Rout} = 2 \times 10^{3}\,\Omega$$

For unbypassed Example (Case 3, RE1 = 990.1 Ω, β = 100)

$$\text{Rbin} := r_{\pi 100} + (\beta\text{low} + 1)\cdot 990.1\cdot\Omega \qquad \text{Rbin} = 1.052 \times 10^{5}\,\Omega$$

$$\text{Rin} := \frac{1}{\frac{1}{\text{Rbin}} + \frac{1}{\text{R1}} + \frac{1}{\text{R2}}} \qquad \text{Rin} = 9.134 \times 10^{3}\,\Omega$$

$$\text{Rout} := \text{RC} \qquad \text{Rout} = 2 \times 10^{3}\,\Omega$$

Conclusions:

- **Full Emitter Bypassing: Highest A_{VT} but most dependent upon β. Lowest Rin.**
- **No Emitter Bypassing: Smallest A_{VT} but least dependent upon β. Highest Rin**
- **Partial Emitter Bypassing: Yields a tradeoff between size of A_{VT} and β stability. Moderately high Rin.**

General Voltage Amplifier Model

This model holds for all voltage amplifiers, be they BJT, FET, Vacuum Tube, OP-AMP. This model is DIFFERENT from the BJT model we have used thus far. Its parameters are Rin, Rout, and Avo (unloaded voltage gain).

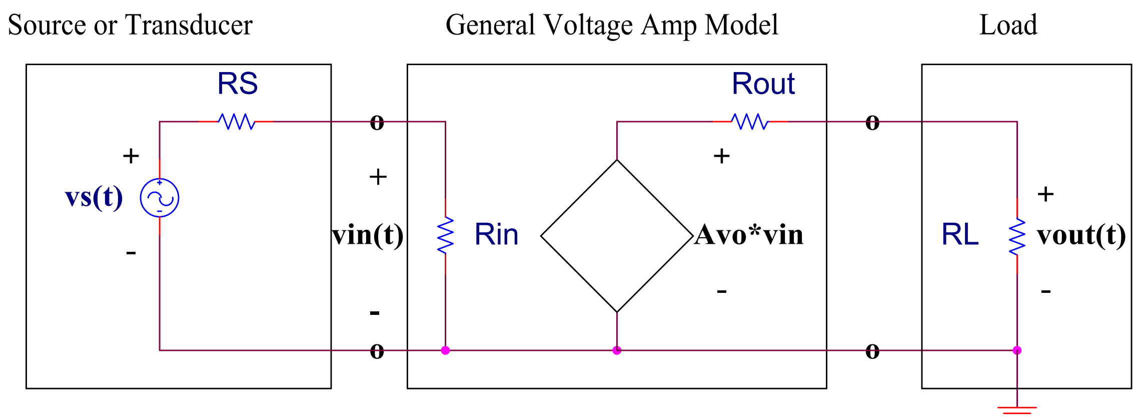
Note that this model uses a voltage-controlled voltage source, rather than a current-controlled current source, as in the BJT model.

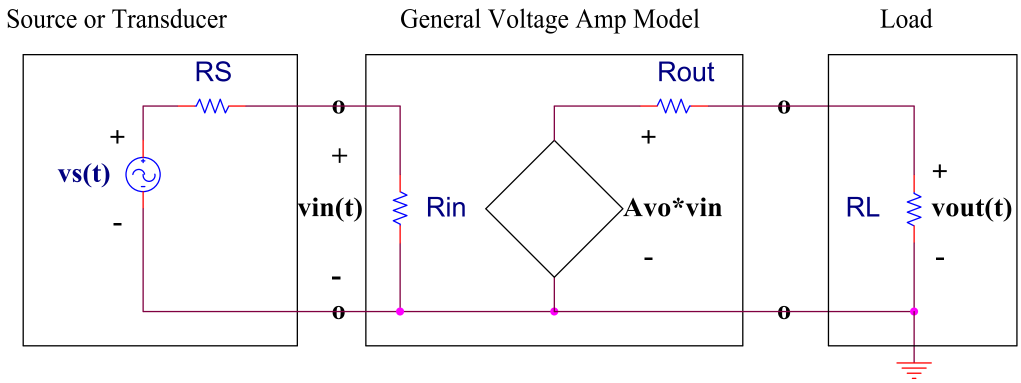
We shall see that this model allows us to very easily find Av = vout/vs or Av_T = vout/vin for an amplifier with arbitrary source termination (RS) and load termination (RL) by application of the voltage divider equation.

Let us define Avo as the "unloaded", or "open circuit" voltage gain

Avo = **vout/vin)$_{RL=\infty}$**

General Voltage Amplifer with Source termination RS and Load termination RL





Overall Voltage Gain:

Av = vout/vs = (vin/vs)*(Avo*vin)/vin*(vout/Avo*vin)

= Rin/(RS+Rin)*Avo*RL/(Rout+RL)

Transducer Voltage Gain (directly measurable in laboratory):

Av_T = vout/vin = (Avo*vin)/vin*(vout/Avo*vin)

= **Avo*RL/(Rout+RL)**

Returning to our Fully-Bypassed CE Amplifier Example

Let us assume that

RE1 = 0 Ω, R1 = 27.8 kΩ, R2 = 15.63 kΩ
RE = 990 Ω, RC = 2 kΩ, RL = 4 kΩ,
RS = 1 kΩ, and β = 100

For the Fully Bypassed Example (RE1 = 0 Ω)

First find the unloaded voltage gain (with RL set to infinity

$$Avo := \frac{-\beta}{r_\pi} \cdot RC \qquad Avo = -38.462$$

$$Rbin := r_\pi \qquad Rin := \frac{1}{\frac{1}{Rbin} + \frac{1}{R1} + \frac{1}{R2}}$$

$$Rin = 3.421 \times 10^3 \, \Omega$$

$$Rout := R_C \qquad Rout = 2 \times 10^3 \, \Omega$$

$$Av := \frac{Rin}{R_S + Rin} \cdot Avo \cdot \frac{R_L}{R_L + Rout} \qquad Av = -19.842$$

$$Av_T := Avo \cdot \frac{R_L}{R_L + Rout} \qquad Av_T = -25.641$$

For the partially-bypassed example $RE1 := 50 \cdot \Omega$

$$Avo := \frac{-\beta}{r_\pi + (\beta + 1) \cdot RE1} \cdot R_C \qquad Avo = -19.512$$

$$Rbin := r_\pi + (\beta + 1) \cdot RE1 \qquad Rin := \frac{1}{\frac{1}{Rbin} + \frac{1}{R1} + \frac{1}{R2}}$$

$$Rin = 5.062 \times 10^3 \, \Omega$$

$$Rout := R_C \qquad Rout = 2 \times 10^3 \, \Omega$$

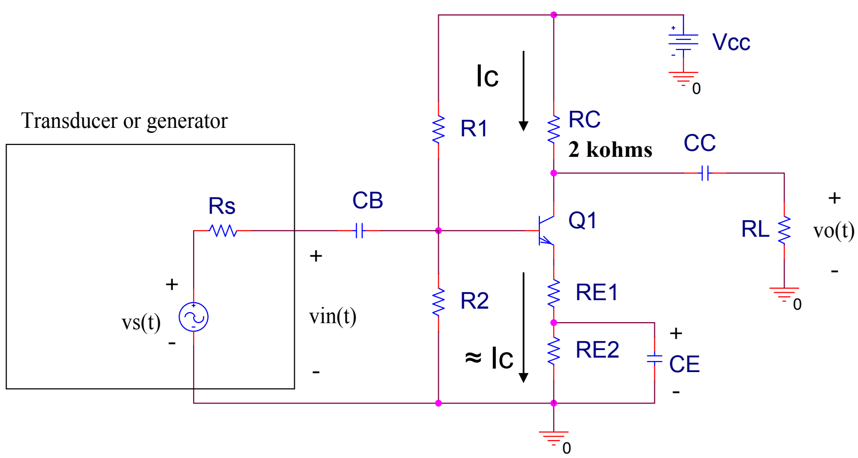
$$Av := \frac{Rin}{R_S + Rin} \cdot Avo \cdot \frac{R_L}{R_L + Rout} \qquad Av = -10.862$$

$$Av_T := Avo \cdot \frac{R_L}{R_L + Rout} \qquad Av_T = -13.008$$

DC and AC Load Lines

Maximum Symmetrical Vce(t) Output Voltage Swing

-Finding the largest permissible sinusoidal output voltage swing



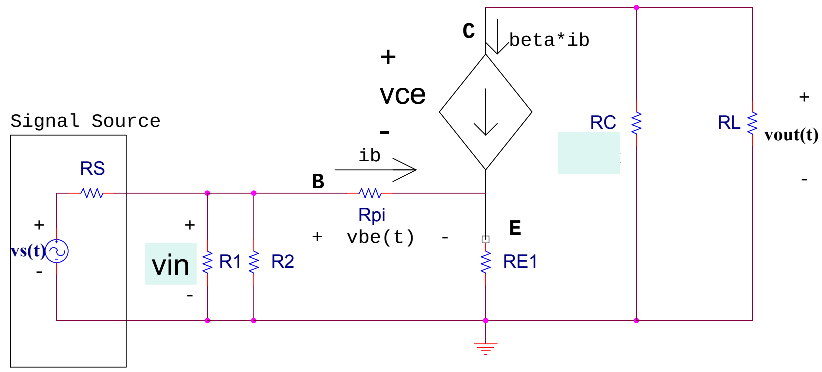
From DC Model, a KVL equation around collector loop yields

Vcc = Ic*RC+Vce+(Ic/β)(β+1)*RE ≈ Ic*RC+Vce+Ic*RE (Recall RE = RE1+RE2)

Vcc = Ic*(RC + RE) + Vce

⇒Ic = -1/(RC+RE)*Vce + Vcc/(RC + RE)

Thus Ic vs. Vce DC load line has Ic intercept of Ic = Vcc/(RC+RE), a slope of -1/(RC+RE), and a Vce intercept of Vce = Vcc



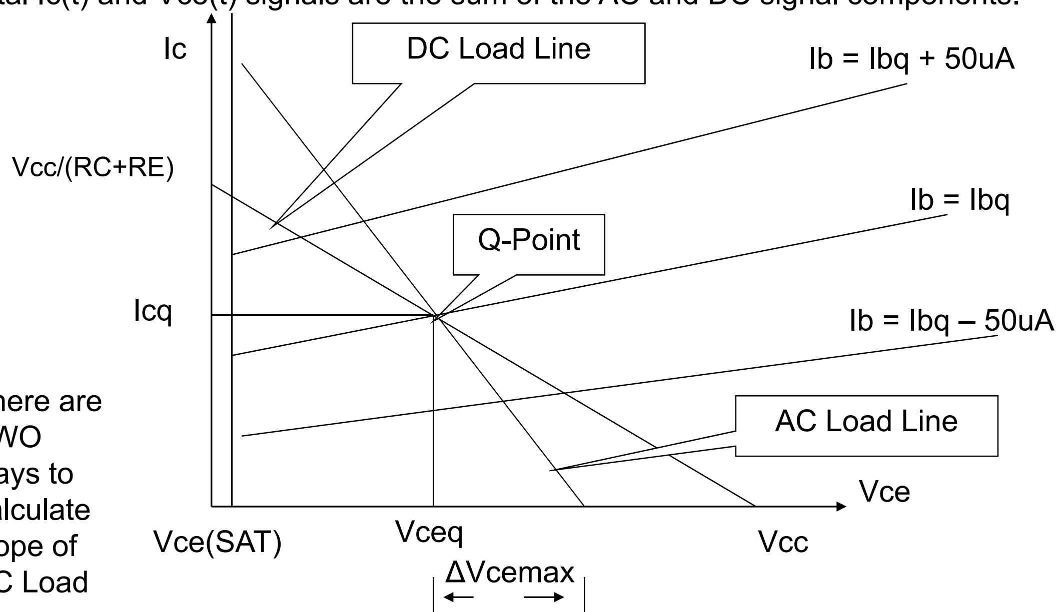
In the AC model of this circuit, where Vcc has been set to zero, and capacitors CC and CE have become short circuits, a KVL equation around the collector loop reveals (Assuming : ie ≈ ic)

$$0 = ic(t)*(RC // RL) + vce(t) + RE1*ic(t)$$

$$ic = -vce/(RE1 + (RC // RL))$$

Thus the slope of the AC load line is 1/ (RE1 + (RC // RL)), which is considerably steeper than slope of the DC load line, -1/(RE + RC)

The AC and DC load lines must both pass through the DC bias Q-point, since the total Ic(t) and Vce(t) signals are the sum of the AC and DC signal components.



There are TWO ways to calculate slope of AC Load Line:

Slope AC Load Line = -1/((RC // RL) + RE1) = -Icq / ΔVcemax

We may solve for ΔVcemax. For our fully-bypassed example (RE1 = 0),

$$\Delta Vcemax = Icq*((RC // RL) + RE1)$$

$$= (1\ mA)*(2k // 4k) = 1.33\ V$$

Thus the Vce(t) total (dc + ac component) output voltage signal may swing ***above*** the Q-point value "Vceq" by ΔVcemax = 1.33 V before the BJT enters cutoff and stops amplifying. Likwise, Vceq may swing ***below*** the Vceq by (Vceq – Vce(SAT)) volts = 2 – 0.2 = 1.8 V before it hits saturation and stops amplifying. Because the output voltage is typically thought to swing symmetrically (sinusoidally) about the Q-point, just as much above the Q-pt as below it, we must take the smaller of these two distances. Because

ΔVcemax = 1.33 V < (Vceq – Vce(SAT)) = 1.8 V

We take our Maximum Symmetrical Vce(t) Output Voltage Swing to be

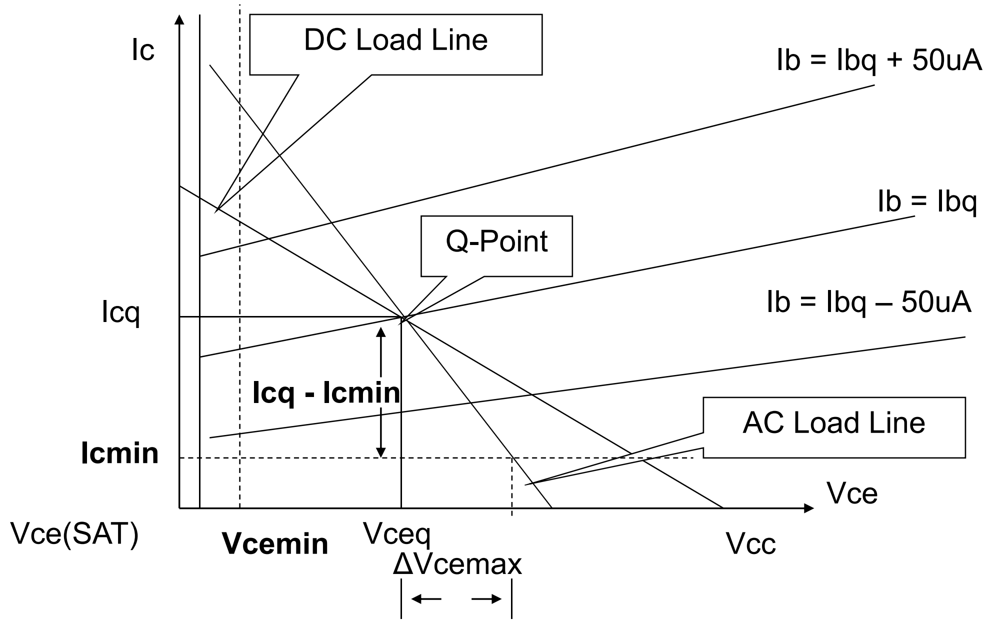
Max. Symm Vce Swing = 2*(ΔVcemax) = 2(1.33) = 2.66 V, peak-to-peak.

If the above inequality were reversed, as it sometimes is, then

Max. Symm Vce Swing = 2*((Vceq – Vce(SAT)) (in **V, peak-to-peak**)

Note: Take the smaller distance and double it – since "*a chain is only as strong as its weakest link*"

Sometimes a "margin for error" is allowed for, by not allowing Vce to rise so far as to allow Ic to hit zero, but rather requiring Ic to remain above a certain specified minimum value "Icmin" that is slightly above 0. This is especially desirable because the BJT's β decreases markedly as Ic comes close to 0, and thus this guarantees a more linear amplifying range. Likewise, Vce may not be allowed to fall so far as to reach saturation, where Vce = Vce(SAT). Instead, Vce might be restricted to lie above a specified minimum Vce value "Vcemin" that is slightly above Vce(SAT). The modified procedure is outlined on the next slide:



Slope AC Load Line = -1/((RC // RL)+RE1) = -(Icq – Icmin)/ ΔVcemax

Solve for ΔVcemax = distance Vce can swing ABOVE Vceq

Calculate (Vceq – Vcemin) = distance Vce can swing BELOW Vceq

Take whichever distance is SMALLER, double it, and that predicts the Maximum Symmetrical Vce Swing

Example 1 (Consider the Fully Bypassed Case => RE1 = 0)

Let us assume that the following constraints have been specified:

Vcemin = 0.4 V and Icmin = 0.1 mA

Then the distance Vce may swing above Vceq is

-1/((RC // RL)+RE1) = -(Icq – Icmin)/ ΔVcemax => **ΔVcemax = 1.2 V**

The distance Vce may swing below Vceq is

Vcq – Vcemin = 2 – 0.4 = 1.6 V

Because 1.2 V < 1.6 V, the Max Symm Swing is 2(1.2) = 2.4 V peak-peak

Example 2 Again consider the Fully Bypassed Case => RE1 = 0; but this time, assume RL has been removed; RL = ∞

Let us assume that same constraints as in Example 1:

Vcemin = 0.4 V and Icmin = 0.1 mA

Then the distance Vce may swing above Vceq is

-1/(RC+RE1) = -(Icq – Icmin)/ ΔVcemax => **ΔVcemax = 1.8 V**

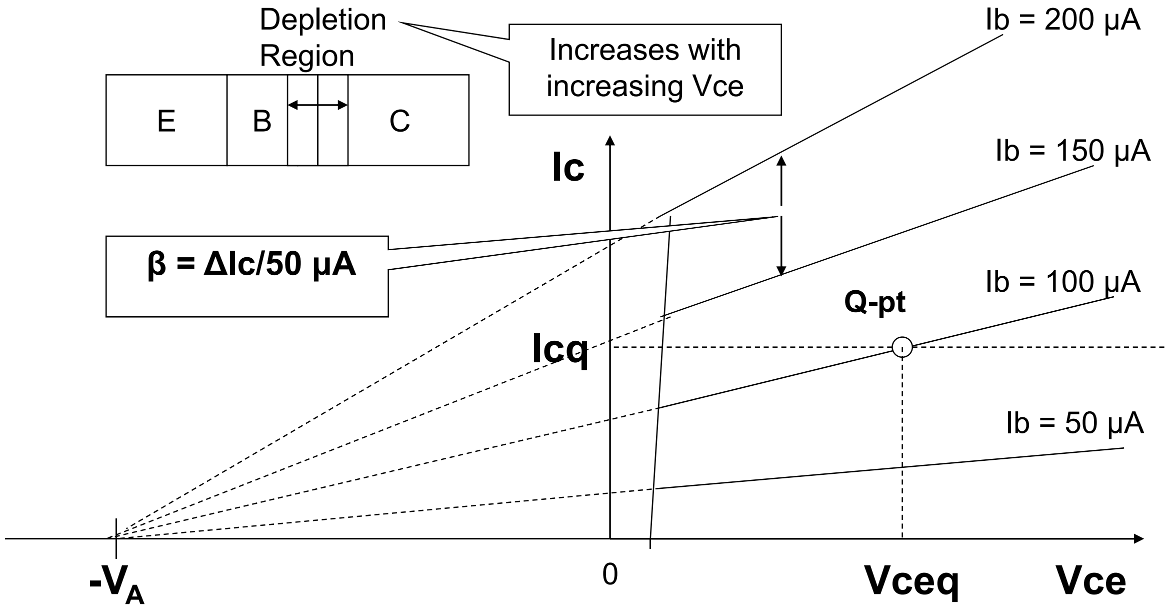
The distance Vce may swing below Vceq is

Vcq – Vcemin = 2 – 0.4 = 1.6 V

Because 1.6 V < 1.8 V, the Max Symm Swing is 2(1.6) = 3.2 V peak-peak.

Note that in the first example the Max Symm Swing was limited by the amount Vce could RISE above Vceq, while in the second example, the Max Symm Swing was limited by the amount Vce could FALL below Vceq!

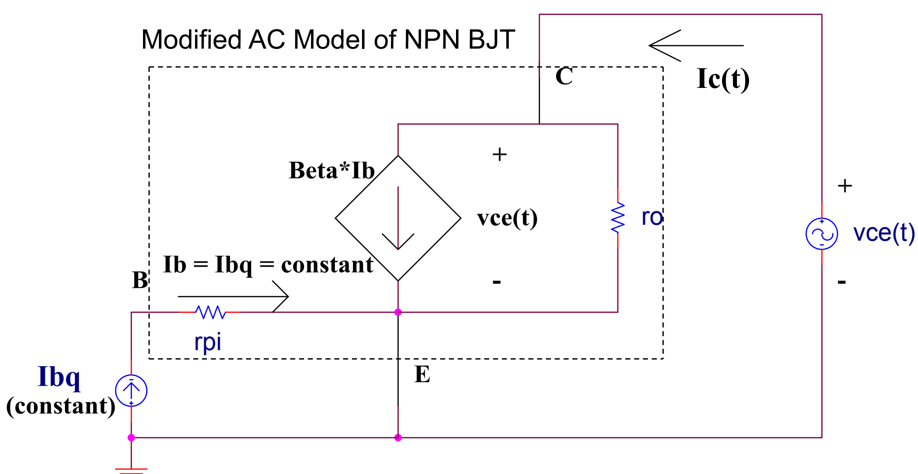
Including the effects of Base-Width Modulation (also called the "Early Effect", V_A) in the AC Model of the NPN BJT: The BJT's output resistance "ro" parameter



Note **β = ΔIc/ ΔIb increases with increasing Vce because as Vce increases the width of the reverse-biased depletion region increases, making the effective width of the base region thinner. The thinner the base region, the closer α is to 1.0, so β= α/(1- α) becomes larger.**

Assuming Ib(t) = Ibq = constant, and thus the controlled current source "pumps" constant current = β*Ibq. Then as Vce(t) is varied, an Ic vs. Vce curve is obtained that passes through the Q-point, whose (slight) upward slope may be accounted for in the AC model of the BJT by placing a high value of resistance (ro) across the controlled-current source in the BJT's AC model, as shown below:

Ic = β*Ibq + Vce(t)/ro



Because in the forward-active region,

$$Ic = \beta * Ibq + vce(t)/ro$$

It should be apparent that the forward-active portion of the Ic vs. Vce curve should be linear (of the form y = mx + b), and have a slope = 1/ro.

Note from the previous slide that another way of calculating this slope is in terms of the Early voltage parameter, V_A:

$$\text{Slope} = 1/ro = Icq/(V_A+Vceq)$$

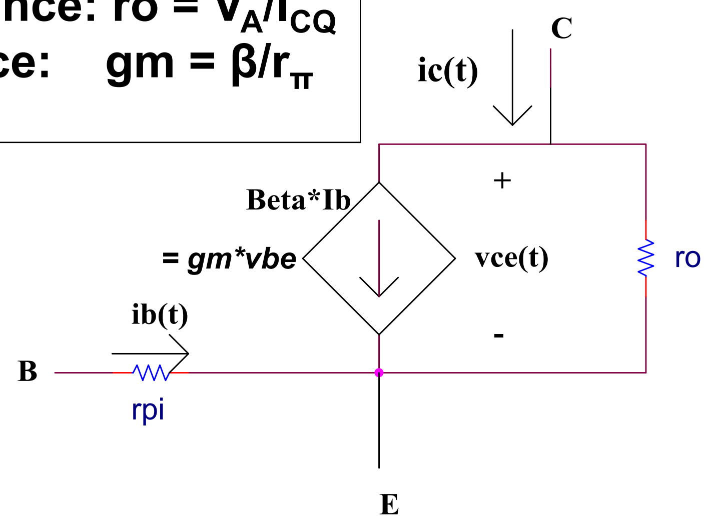
Furthermore, because 50 V < VA < 200 V, Vceq is typically on the order of several volts, we may drop Vceq from the following expression:

$$1/ro = Icq / V_A \quad =>$$

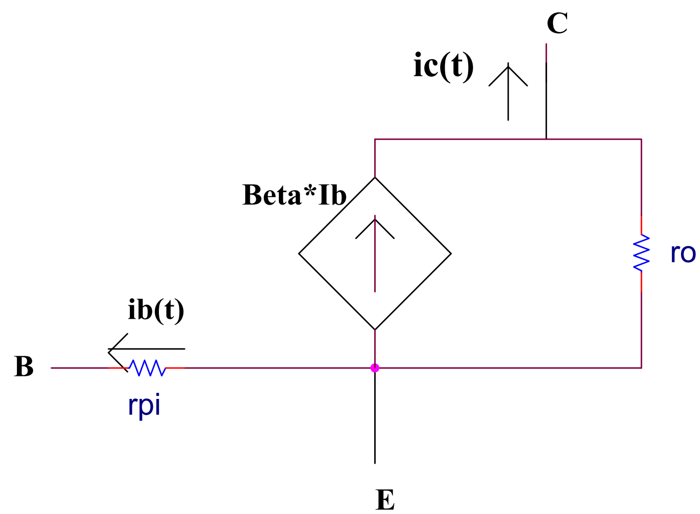
$$ro = V_A/Icq$$

Improved Forward-Active NPN BJT AC Small-Signal "Hybrid π" Model

AC base resistance $r_\pi = \eta V_T/I_{BQ}$
AC output resistance: $ro = V_A/I_{CQ}$
Transconductance: $gm = \beta/r_\pi$



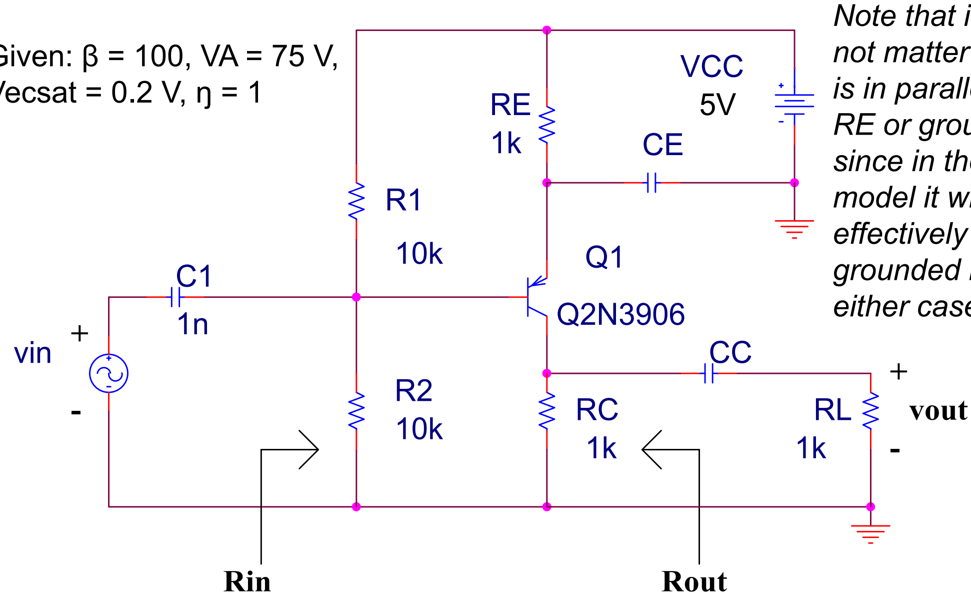
AC "Hybrid-π" Model of Forward-Active PNP BJT



Note that the AC Models of the NPN and PNP BJT are actually *equivalent*, as we can see by reversing all current reference directions.

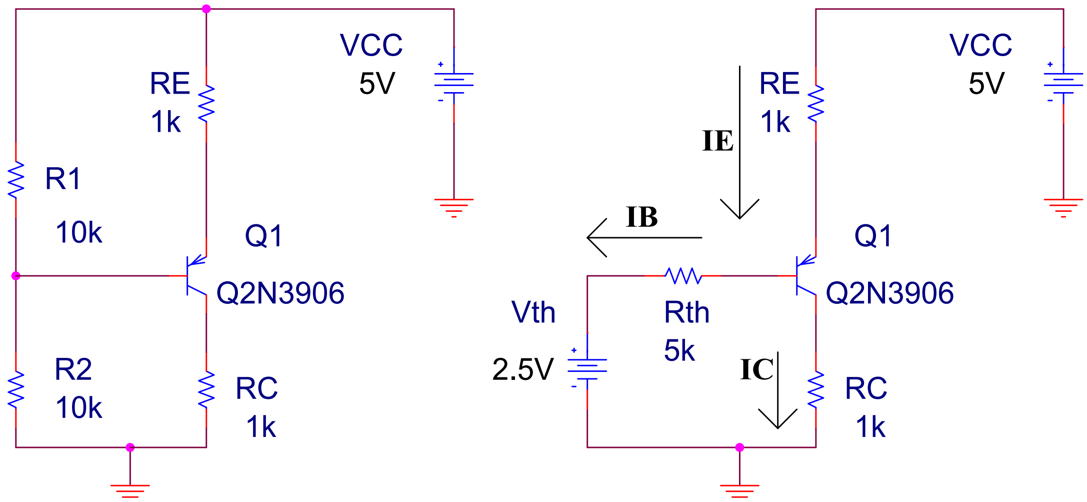
Example: PNP BJT CE Amplifier Analysis

Given: β = 100, VA = 75 V, Vecsat = 0.2 V, η = 1



Note that it does not matter if CE is in parallel with RE or grounded, since in the AC model it will be effectively grounded in either case.

DC Model before and after source Theveninization



To find IB, write a KVL equation Around Base Loop. *Remember this is PNP BJT!*

Vcc = (β+1)IB*RE + VEBon + Rth*IB+Vth

=> **5 = 101*Ib*1k + 0.7 + 5k*Ib + 2.5** => ***IB = 16.98 μA***

VEC = (Vcc – (β + 1)Ib*RE) – β*IB*RC

= (5-101**16.98 μA*1k) – 100*16.98 μA*1k*

= 1.587 V > VECsat => BJT Fwd Active, as assumed

*IC = IB** β = 16.98 *μA * 100 = 1.698 mA*

Q-point of the PNP BJT is (VEC = 1.587 V, IC = 1.698 mA)

Now that the DC analysis is complete, we can calculate the small-signal ac (hybrid-π) model parameters

$r_\pi = \eta V_T/I_{BQ}$ = (1*26 mv) / 16.98 *μA* = *1.53 kΩ*

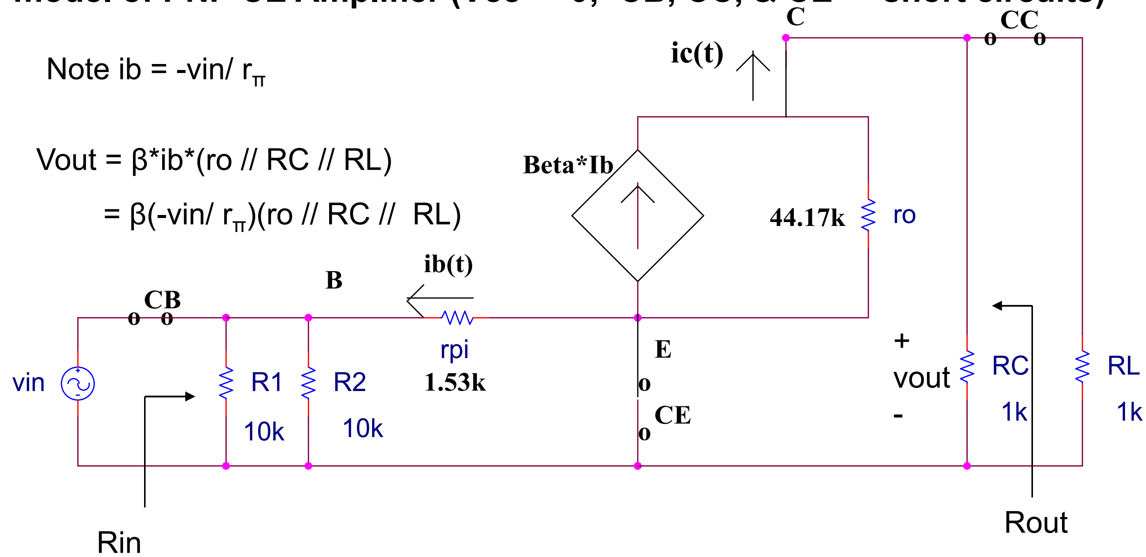
ro = V_A/I_{CQ} = 75 V / 1.698 *μA* = 44.17 kΩ

AC model of PNP CE Amplifier (Vcc -> 0; CB, CC, & CE -> short circuits)

Note ib = -vin/ r_π

Vout = β*ib*(ro // RC // RL)

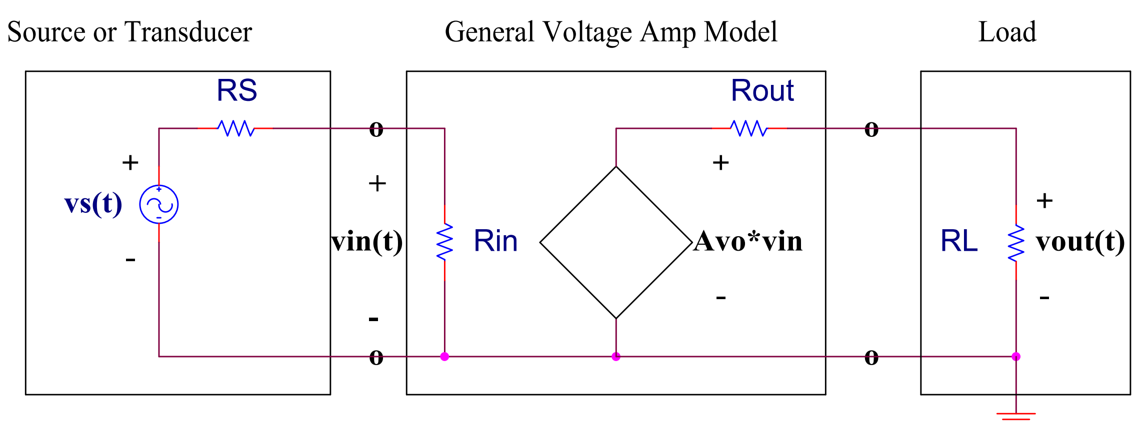
= β(-vin/ r_π)(ro // RC // RL)



Rout = Rc // ro = 1 kΩ // 44.17 kΩ = 977.9 Ω

Rin = R1 // R2 // r_π = 10 kΩ // 10 kΩ // 1.53 kΩ = 1.17 k Ω

Avo = -β(Rc // ro)/ r_π = -100(1 kΩ // 44.17 kΩ)/1.53 kΩ = -63.9



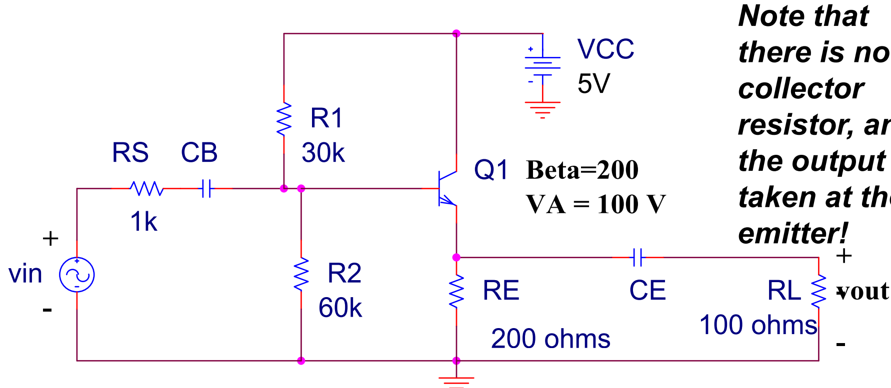
In this case, RS = 0,

so Avt = Av = vout/vin = Avo*(RL/(Rout+RL)

Av = -63.9*(1k/(1kΩ + 977.9 Ω) = -32.3

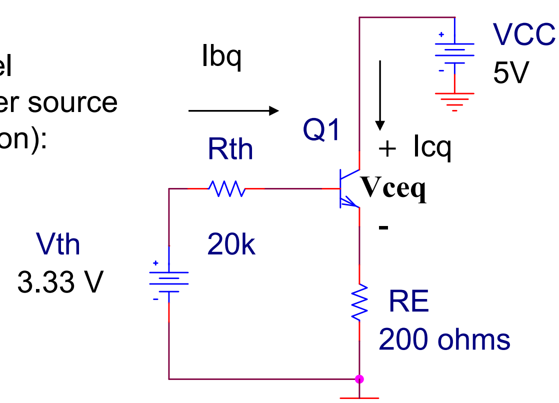
Common-Collector (also called Emitter Follower) BJT Amplifier

Same 3-resistor biasing network and DC model as before, but now the output is taken across the (unbypassed) emitter resistor, so the AC model changes dramatically.



Note that there is no collector resistor, and the output is taken at the emitter!

The DC Model becomes (after source Theveninization):



$$I_{bq} = \frac{V_{th} - 0.7}{R_{th} + (\beta+1)R_E}$$

$$= \frac{3.33\text{ V} - 0.7\text{ V}}{20\text{k} + 201 \cdot 200}$$

$$= \underline{43.7\ \mu\text{A}}$$

Vceq = Vcc – (β + 1)Ibq*RE = <u>3.24 V</u>

> Vce(SAT) => Our assumption of forward-active mode is valid

Icq = β*Ib = 200*(43.7 μA) = <u>8.74 mA</u>

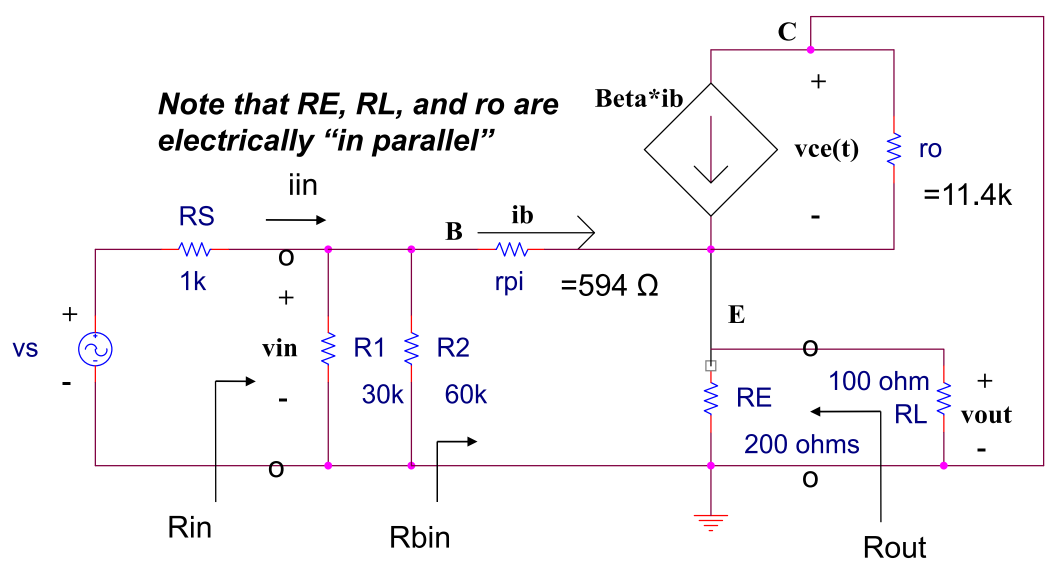
Now that the dc analysis is complete, we can find r_π and ro

$r_\pi = n*V_T/Ibq$ = (1)(26 mV)/ 43.7 μA = *594.4 Ω* Assume IC BJT (n=1)

ro = VA / Icq = 100 V / 8.74 mA = <u>11.44 kΩ</u>

Now it is time to construct the AC model of the CC (Emitter Follower) amplifier:

AC Model of CC (Emitter Follower) Amplifier



Find Avo (Remove RL)

Remember to REMOVE RL

When finding Avo!

KVL around base loop =>

$$vin = ib \cdot r\pi + (\beta + 1) \cdot ib \cdot \left(\frac{RE \cdot ro}{RE + ro} \right)$$

=> $$ib = \frac{vin}{r\pi + (\beta + 1) \cdot \frac{RE \cdot ro}{RE + ro}}$$

KVL around emitter loop =>

$$vout = (\beta + 1) \cdot ib \cdot \frac{RE \cdot ro}{RE + ro}$$

$$vout = (\beta + 1) \cdot \frac{vin}{\left[r\pi + (\beta + 1) \cdot RE \cdot \frac{ro}{(RE + ro)} \right]} \cdot RE \cdot \frac{ro}{(RE + ro)}$$

Substituting ib equation into vout yields:

$$Avo = \frac{vout}{vin} = \frac{(\beta + 1) \cdot \frac{RE \cdot ro}{RE + ro}}{r\pi + (\beta + 1) \cdot \frac{RE \cdot ro}{RE + ro}}$$

=(β+1)(RE //ro) / (rπ + (β+1)(RE // ro))

Note that Avo can never be > 1 **, and Avo is approximately = 1 if**

(β+1)*(RE // ro) >> r_π

In our example

$$Avo := \frac{(\beta + 1) \cdot \frac{RE \cdot ro}{RE + ro}}{r\pi + (\beta + 1) \cdot \frac{RE \cdot ro}{RE + ro}} \qquad Avo = 0.985$$

The input resistance Rbin may be found by writing a KVL loop around the base loop with RL *re-inserted* in the circuit.

$$vin = r\pi \cdot ib + (\beta + 1) \cdot ib \cdot \left(\frac{1}{\frac{1}{RE} + \frac{1}{ro} + \frac{1}{RL}} \right)$$

$$Rbin = \frac{vin}{ib} = r\pi + (\beta + 1) \cdot \left(\frac{1}{\frac{1}{RE} + \frac{1}{ro} + \frac{1}{RL}} \right)$$

Note that, unlike the CE amplifer, Rbin for the CC amplifier depends upon the value of load resistance, RL.

In our example, $Rbin := 13.92 \cdot k\Omega$

$$Rin := \frac{1}{\frac{1}{R1} + \frac{1}{R2} + \frac{1}{Rbin}}$$

$Rin := 8.208 \cdot k\Omega$

Note that, compared to RE and RL, Rin is a fairly large input resistance. It can be made larger if R1 and R2 are made larger, though this increases the dependence of the Q-point on β.

The input resistance Rbin "with RL removed" will be needed later:

$$vin = r\pi \cdot ib + (\beta + 1) \cdot ib \cdot \left(\frac{1}{\frac{1}{RE} + \frac{1}{ro}} \right)$$

$$Rbin\_no\_RL = \frac{vin}{ib} = r\pi + (\beta + 1) \cdot \left(\frac{1}{\frac{1}{RE} + \frac{1}{ro}} \right)$$

Note that, unlike the CE amplifer, Rbin for the CC amplifier depends upon the value of load resistance, RL.

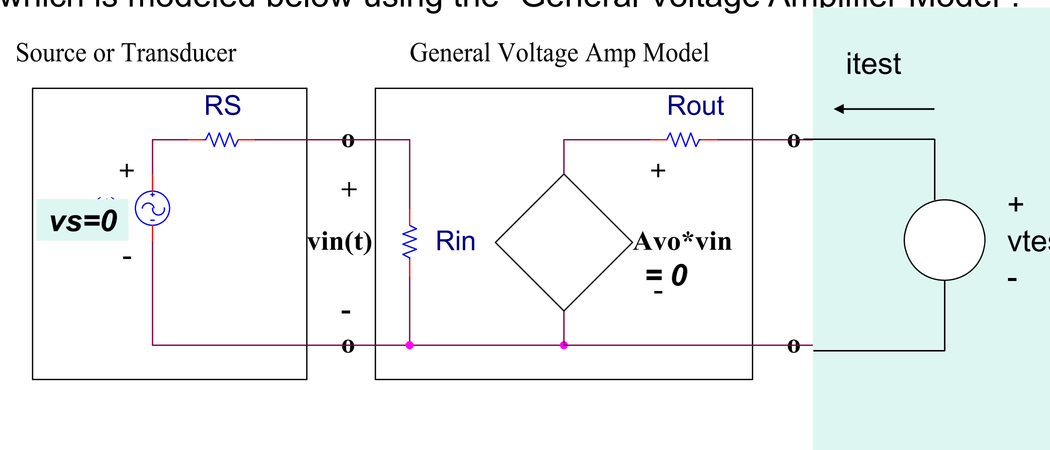
In our example, $Rbin\_no\_RL := 40.1 \cdot k\Omega$

$$Rin\_no\_RL := \frac{1}{\frac{1}{R1} + \frac{1}{R2} + \frac{1}{Rbin\_no\_RL}}$$

$$Rin\_no\_RL = 1.334 \times 10^{4} \Omega$$

Rin with RL removed is used in the general voltage amplifier model of the CC amplifier

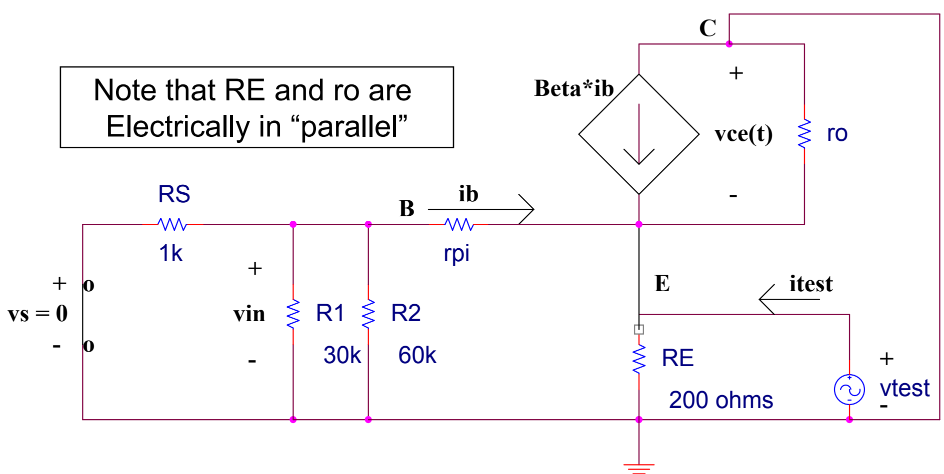
Finding Rout for the CC amplifier is *more complicated* than it was for the CE amplifier case, where we found Rout = RC. With a small ac test voltage source connected across the output terminals of the CC amplifier, which is modeled below using the "General Voltage Amplifier Model":



It should be clear that

$$\textbf{Rout} = (vtest/itest)_{vs\,=\,0}$$

Applying this ac test voltage source to the AC model of the CC BJT circuit (***making sure to set vs = 0***) yields:



KCL at emitter node: -ib - βib - itest + vtest/RE + vtest/ro) = 0

Also, note that ib may be calculated in terms of vtest:

ib = -vtest / (rpi + R1 // R2 // RS)

Substituting this expression for ib into the KCL equation yields

(β+1)vtest / (rpi + R1 // R2 // RS) - itest + vtest/RE + vtest/ro = 0

=> vtest{(β+1)/ (rpi + R1 // R2 // RS) + 1/RE + 1/ro} = itest

Rout = vtest / itest

= 1/{1/[(rpi + R1 // R2 // RS) / (β+1) + 1/RE + 1/ro]}

= {RE // ro} // {(rpi + R1 // R2 // RS) / (β+1)}

$$Rout := \cfrac{1}{\cfrac{1}{\cfrac{1}{\frac{1}{RE}+\frac{1}{ro}}} + \cfrac{1}{\cfrac{\left[\cfrac{1}{\left(\frac{1}{R1}+\frac{1}{R2}+\frac{1}{RS}\right)}+r\pi\right]}{\beta+1}}}$$

In our example, with RS = 1k,
Rout = 196.6 // [1.55k/(β+1)]
Rout = 7.41 Ω

Ro relatively low; & depends upon RS

Note how the "reflection rule" Is used in reverse. The equiv resistance In the base circuit is Is divided by **(β+1)**

CC Amplifier Summary

$$\mathbf{Avo} = \frac{(\beta+1)(RE\ //\ ro)}{r_\pi + (\beta+1)(RE\ //\ ro)}$$

Note: Avo is slightly less than 1.0

Rbin = r_π + (β+1)(RE // ro // RL)
Rbin_no_RL = r_π + (β+1)(RE // ro)
Rin = (Rbin // R1 // R2)

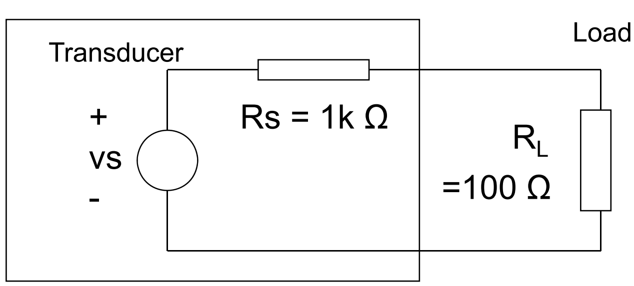
Note: Rin is relatively high. It depends Upon RL, so the general voltage amplifier model is NOT independent of output termination as it is for the CE amplifier.

Rout = (RE // ro) // (r_π + R1 // R2 // RS) / (β+1)

Note: Rout is relatively low. It depends upon RS, so the general voltage amplifier model is NOT independent of input termination, as it is for the CE amplifier

But what good is the CC (Emitter Follower) Amplifier, since it has a voltage gain that is slightly less than unity? What advantage does this amplifier have over a wire that connects input to output?

Consider a situation where a transducer with open-circuit voltage vs and output resistance Rs=1kΩ that must deliver a signal across a R_L=100 Ω load

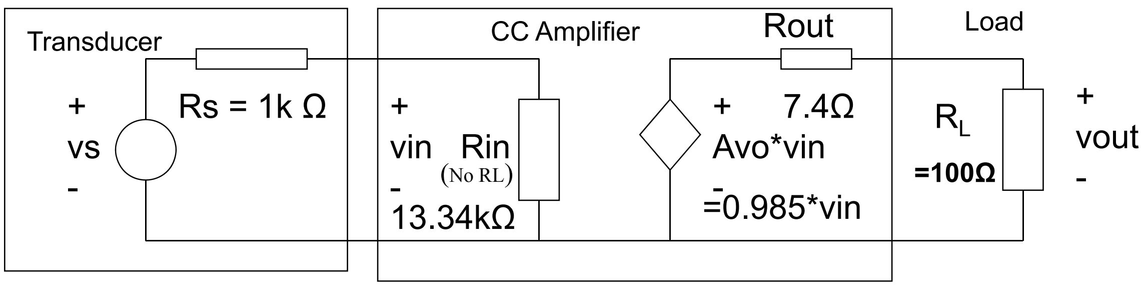


+
vout = vs*R_L/(Rs+R_L)
-
= vs*(100/(100+1000)
= vs/11 = 0.091*vs

<u>Only 9.1% of the available transducer voltage (vs) is delivered to the load!</u>

<u>We say that the transducer's output has been severely "loaded" by R_L</u>

This "loading" problem may be solved by placing the CC (Emitter Follower) amplifier that we have just designed between the transducer and the load:



Now vout=vs*Rin_no_RL/(Rin_no_RL+Rs)*Avo*RL/(Rout+RL)

=vs*(13.34/(1+13.34)*0.985*(100/(7.4+100) = 0.853*vs

Now 85.3% of the available transducer voltage is delivered to the load!

Note that there is a <u>very subtle</u> difference in applying the general voltage amplifier model for the CC Amplifier.

This difference is due to the fact that in a CC amplifier, Rin depends upon RL.

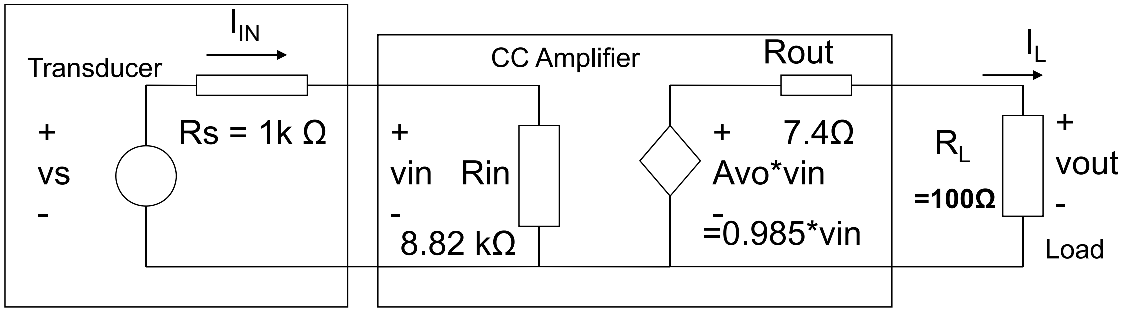
When finding the loaded voltage gain (Av) using the general voltage amplifier model, we must use the value of Rin with RL removed ("Rin_no_RL").

This is because we are calculating the strength of the "***<u>open-circuit" voltage source</u>*** "Avo*vin". Because it must represent the ***<u>open circuit</u>*** voltage at that point in the circuit, it must be calculated assuming that no load has yet been placed across the output terminals:

Avo*vin = Avo*vs*(Rin_no_RL/(Rin_no_RL+Rs)

Thus, the overall loaded voltage gain is calculated as

Av = Rin_no_RL/(Rin_no_RL+Rs)*Avo*RL/(Rout+RL)



While the CC amplifier exhibits a voltage gain slightly less than 1, it exhibits a *much higher* current gain and power gain. Let us define ***current gain*** as

$A_I = I_L/I_{IN}$

$= (vout/R_L) / (vs/(Rs+Rin)) = (vout/vs)*(Rs+Rin)/R_L$

$= Av*(Rs+Rin)/R_L$

When calculating A_I, the actual loaded value of Rin is used!

Note A_I is expressed in terms of A_V (not A_{VO})

Likewise let us define ***power gain*** as

$A_P = Pout/Pin = (vout*I_L)/(vs*I_{IN}) = (vout/vs)*(I_L/I_{IN}) = A_V*A_I$

In this example,

Av = vout/vs

= Rin_no_RL/(Rin_no_RL+Rs)*Avo*RL/(Rout+RL)

= (13.34/(13.34+1)*0.985*(100/(7.4+100) = 0.853

A_I = Av*(Rs+Rin)/RL

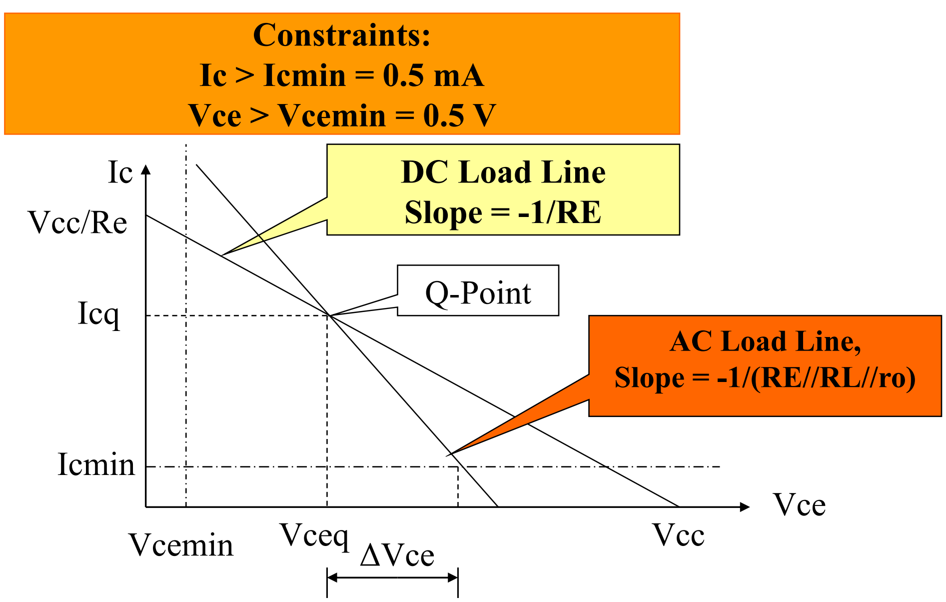
= 0.853*((1kΩ + 8.2kΩ) / 100Ω) = 78.5

A_P = Av*A_I = 0.853*78.5 = 67

Note that a CC amplifier may have a voltage gain slightly less than one, but it has a current gain and a power gain that is usually much greater than one!

Finding Maximum Symmetrical Vce Output Swing for CC Amplifier

(Use our present example)



Slope AC load line = $-1/(RE \mathbin{//} RL \mathbin{//} ro) = -(Icq - Icmin) / \Delta Vce$
$= -1/(200 \mathbin{//} 100 \mathbin{//} 11.4k) = -(8.74\ mA - 0.5\ mA)/ \Delta Vce$

=> $\underline{\Delta Vce = 0.546\ V}$

Thus the amount that Vce may RISE above Vceq is given by

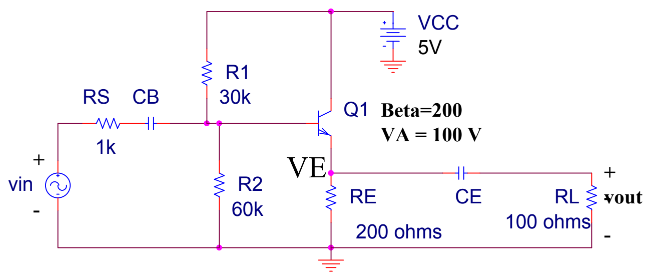
$$\underline{\Delta Vce = 0.546\ V}$$

The amount that vce may FALL below Vceq is given by

$$Vceq - Vcemin = 3.24\ V - 0.5\ V = \underline{2.74\ V}$$

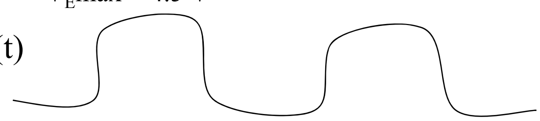
Since 0.549 V < 2.74 V, the amount that Vce RISES is the limiting factor.

Max Symmetrical VCE swing = 2(0.546 V) = <u>1.09 V, peak-peak</u>



$V_E max = 4.5\ V$

$V_E(t)$



$V_E min = 1.21V$

$V_E(t)$ distortion points:

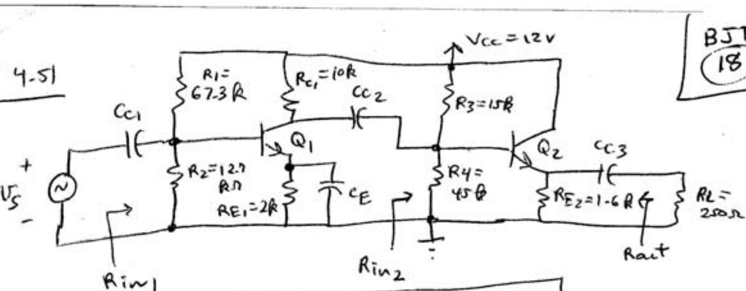
$$V_E max = Vcc - Vcemin = 5\ V - 0.5\ V = \underline{4.5\ V}$$

$$V_E min = Vcc - Vcemax = Vcc - (Vceq + \Delta Vce) = 5\ V - (3.24\ V + 0.546\ V) = \underline{1.21\ V}$$

Cascading two amplifier stages using the general voltage amplifier model

Text 4-51

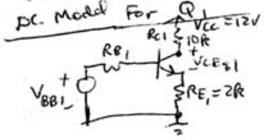
BJT (18)



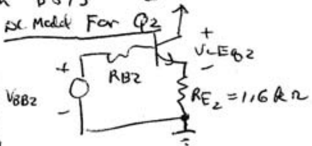
Both BJTs have $\beta_F = 120$, $V_A = \infty$

(a) Find g_m, r_π, r_o for both BJT's

DC Model For Q_1



DC Model For Q_2



$V_{BB_1} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right) = 1.905V$

$R_{B_1} = R_1 \,//\, R_2 = \frac{R_1 R_2}{R_1+R_2} = 10.68\,k\Omega$

KVL around b-e loop $\Rightarrow$

$I_{B_1q} = \frac{V_{BB_1} - 0.7V}{R_{B_1} + (\beta_F+1)R_{E_1}} = 4.77\mu A$

$I_{C_1q} = \beta_F \cdot I_{B_1q} = 0.572mA$

$V_{CEq} = V_{CC} - R_{C_1} I_{C_1q} - (\beta_F+1) I_{B_1q} \cdot R_{E_1}$
$= 5.123V \quad > V_{CEsat} \Rightarrow$ Fwd active!

$V_{BB_2} = V_{CC}\left(\frac{R_4}{R_3+R_4}\right) = 9V$

$R_{B_2} = R_3 // R_4 = \frac{R_3 R_4}{R_3+R_4} = 11.25\,k\Omega$

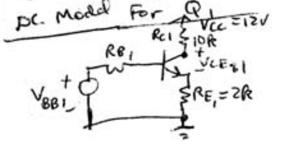
$I_{B_2q} = \frac{V_{BB_2} - 0.7V}{R_{B2} + (\beta_F+1)R_{E2}} = 40.52\mu A$

$I_{C_2q} = \beta_F \cdot I_{B_2q} = 4.862\,mA$

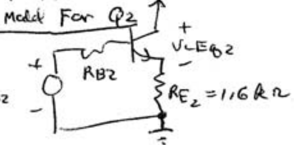
$V_{CE2q} = V_{CC} - (\beta_F+1) I_{B_2q} R_{E_2} = 4.155V$
$> V_{CEsat} \Rightarrow$ Fwd Active!

(a) Find g_m, r_π, r_o for both BJT's

DC Model For Q_1



DC Model For Q_2



$V_{BB_1} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right) = 1.905V$

$R_{B_1} = R_1 \,//\, R_2 = \frac{R_1 R_2}{R_1+R_2} = 10.68\,k\Omega$

KVL around b-e loop $\Rightarrow$

$I_{B_1q} = \frac{V_{BB_1} - 0.7V}{R_{B_1} + (\beta_F+1)R_{E_1}} = 4.77\mu A$

$I_{C_1q} = \beta_F \cdot I_{B_1q} = 0.572mA$

$V_{CEq} = V_{CC} - R_{C_1} I_{C_1q} - (\beta_F+1) I_{B_1q} \cdot R_{E_1}$
$= 5.123V \quad > V_{CEsat} \Rightarrow$ Fwd active!

$V_{BB_2} = V_{CC}\left(\frac{R_4}{R_3+R_4}\right) = 9V$

$R_{B_2} = R_3 // R_4 = \frac{R_3 R_4}{R_3+R_4} = 11.25\,k\Omega$

$I_{B_2q} = \frac{V_{BB_2} - 0.7V}{R_{B2} + (\beta_F+1)R_{E2}} = 40.52\mu A$

$I_{C_2q} = \beta_F \cdot I_{B_2q} = 4.862\,mA$

$V_{CE2q} = V_{CC} - (\beta_F+1) I_{B_2q} R_{E_2} = 4.155V$
$> V_{CEsat} \Rightarrow$ Fwd Active!

For AC Model,

$r_{\pi_1} = \frac{nV_T}{I_{B_1q}} = \frac{1(26mV)}{4.77\mu A} = 5.45\,k\Omega$

$r_{o_1} = \frac{V_A}{I_{C_1q}} = \frac{\infty}{I_{C_1q}} = \infty$

$g_{m_1} \triangleq \frac{i_{c_1}}{v_{be_1}} = \frac{i_{c_1}}{r_{\pi_1} \cdot i_{b_1}} = \frac{\beta_F}{r_{\pi_1}} = 0.022\,\frac{A}{V}$ (s)

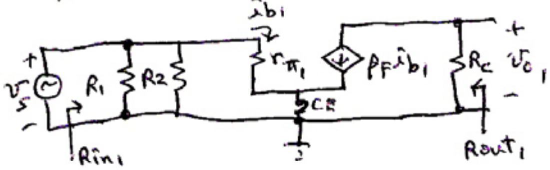
For AC Model

$r_{\pi_2} = \frac{nV_T}{I_{B_2q}} = \frac{(1)(26mV)}{40.52mA} = 641.7\Omega$

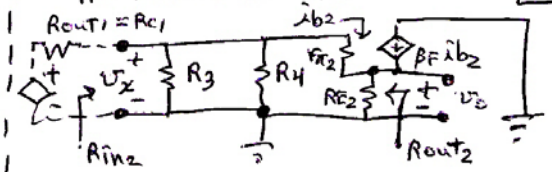
$r_{o_2} = \frac{V_A}{I_{Cq2}} = \frac{\infty}{I_{Cq2}} = \infty$

$g_{m_2} = \frac{\beta_F}{r_{\pi_2}} = 0.1875\,A/V$ (s)

AC Model for Q_1 (CE) Stage



AC Model for Q_2 (CC) Stage



$$R_{in_1} = R_1 // R_2 // r_{\pi_1} = 3.61\,k\Omega$$

$$A_{vo_1} = \frac{-\beta_F}{r_{\pi_1}} R_{c_1} = -220.1$$

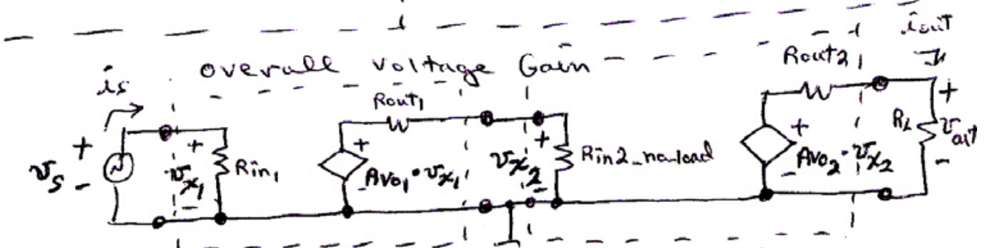
$$R_{out_1} = R_{c_1} = 10\,k\Omega$$

$$R_{in_2\_no\_load} = R_3 // R_4 // [r_{\pi_2} + (\beta_F + 1) R_{E_2}] = 10.63\,k\Omega$$

$$R_{out_2} = R_{E_2} // \frac{(r_{\pi_2} + (R_3 // R_4 // R_{out_1}))}{\beta_F + 1} = 47.6\,\Omega$$

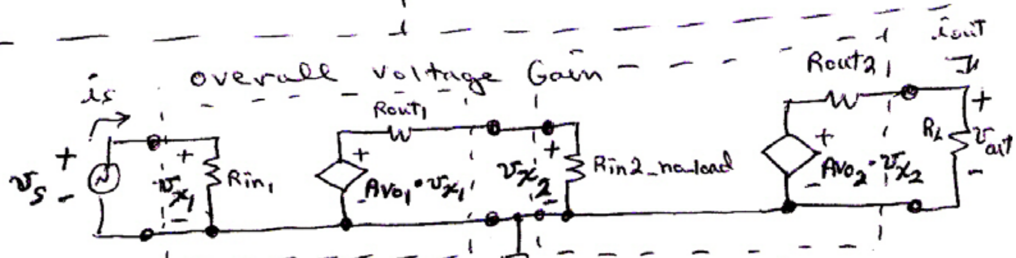
$$A_{vo_2} = \frac{(\beta_F + 1) R_{E_2}}{r_{\pi_2} + (\beta_F + 1) R_{E_2}} = 0.997$$

Overall voltage Gain



$r_{\pi_2} + (\beta_F+1) R_{E_2}$

Overall voltage Gain



$$A_V = \frac{v_{out}}{v_s} = A_{vo_1} \cdot \frac{R_{in2\_no\_load}}{R_{in_2\_no\_load} + R_{out_1}} \cdot A_{vo_2} \cdot \frac{R_L}{R_L + R_{out_2}}$$

$$A_V = -94.9$$

$$A_I = \frac{v_{out}/R_L}{v_s/(R_{in_1})} = A_V \cdot \frac{R_{in_1}}{R_L} = -1370$$

$$A_P = \frac{P_{out}}{P_{in}} = \frac{v_{out} \cdot i_{out}}{v_s \cdot i_s} = A_V \cdot A_I = 1.3 \times 10^5$$

THE END OF BJT Coverage!

(MOSFETs come next)