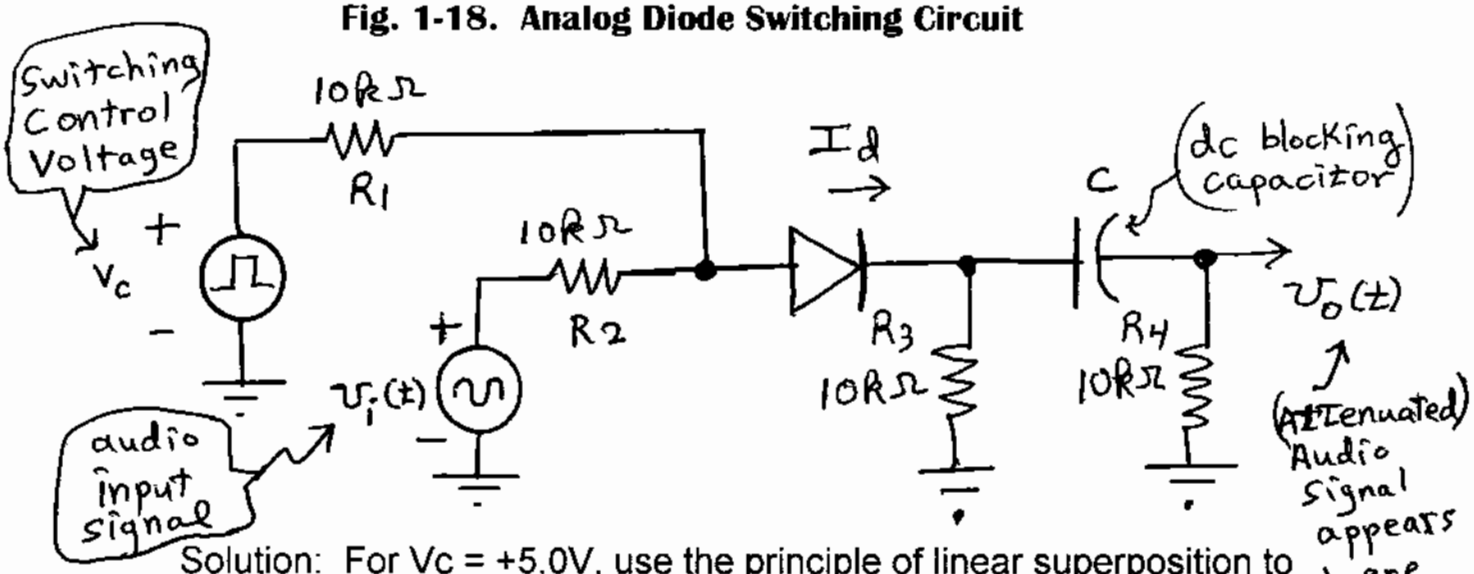
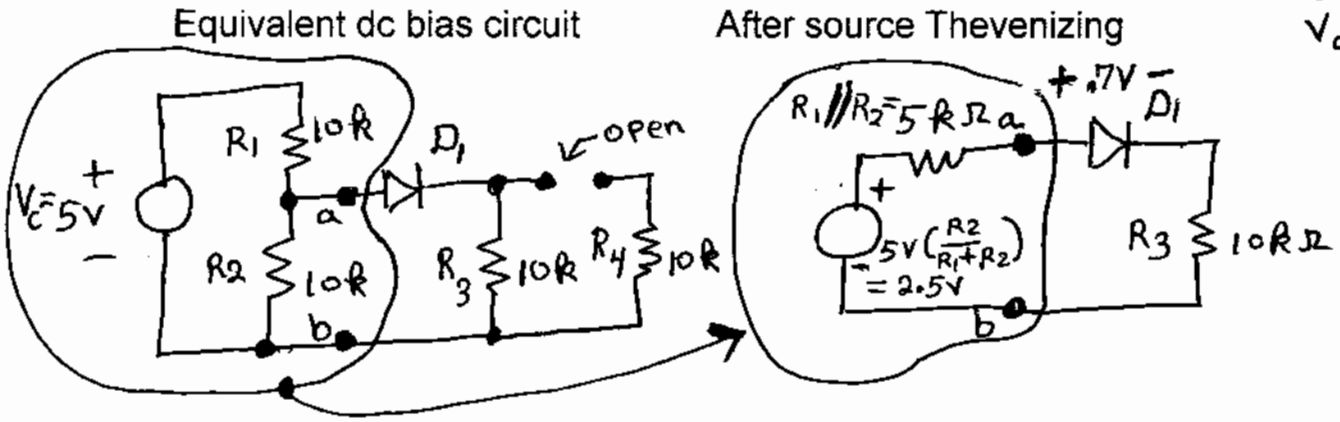
Fig. 1-18. Analog Diode Switching Circuit



Solution: For Vc = +5.0V, use the principle of linear superposition to estimate the dc component of the diode current I_{dc}, assuming the diode model of Fig. 1-17(b). Do this by reducing the ac input signal source vi(t) to zero (replace it with a short circuit). The capacitor C can be replaced by an open circuit, since this is a dc analysis, and at dc a capacitor exhibits infinite impedance. The equivalent circuit is



Therefore, the approximate dc bias current flowing through the diode when Vc = 5.0V is

$$Id := \frac{2.5 - 0.7}{15 \cdot 10^{3}} \qquad Id = 1.2 \cdot 10^{-4} \ \text{A}$$

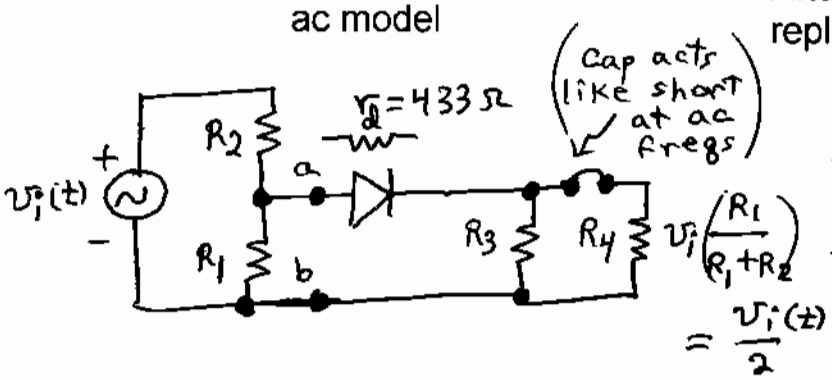
Therefore the ac (small-signal) diode resistance is

$$r = \frac{\eta(0.026)}{I_{dc}} + Rb = \frac{2\cdot(0.026)}{1.2\cdot 10^{-4}} + 0 = 433 \quad \Omega$$

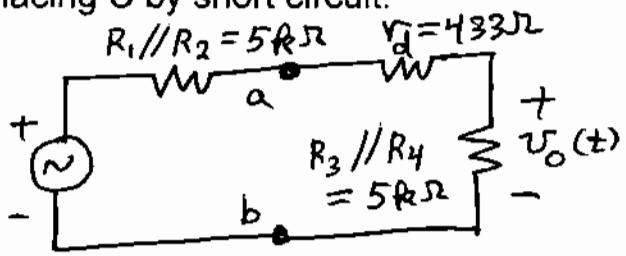
The ac model of the circuit can now be drawn, this time the control source Vc is set to 0 (replaced by a short circuit) and the because the capacitance of capacitor C has been chosen large enough so its ac impedance is small compared to 10kΩ, is also replaced by a short circuit.

Then, the ac model becomes (after source Thevenization):

ac model



After source Thevenization and replacing C by short circuit:



Therefore the ac signal voltage gain may be found using the voltage divider equation:

$$\frac{v_o(t)}{v_i(t)} = \frac{(5000/2)}{5000 + 433.3 - 5000} = 0.479/2 = 0.24$$

Note that for the case when Vc = -5.0 V (analog path OFF), the diode is reverse biased (OFF), and so it behaves as an open circuit in the ac model; thus the ac signal voltage gain vo(t)/vi(t) = 0, as desired.

****

Example 1-7

To show how ***graphical load-line*** analysis allows us to predict the ***dc quiescent operating point*** of a nonlinear circuit element, consider the ***5 V Zener diode voltage regulation circuit*** shown in Fig. 1-18(a). The I-V curve of the Zener diode is shown in Fig. 1-18(b). The Thevenized circuit is shown in Fig. 1-18(c).

$$V_{thev} = 10 \cdot \frac{5}{5 + 1} \qquad R_{thev} = \frac{5 \cdot 10^3 \cdot 1 \cdot 10^3}{5 \cdot 10^3 + 1 \cdot 10^3}$$

$$V_{thev} = 8.333333 \quad V \qquad R_{thev} = 833.333333 \quad \Omega$$

Besides the I-V curve of the nonlinear element (Zener diode) we also have the (linear) I-V curve of the Thevenin equivalent circuit, which may be written (using the same polarities for I and V that were already defined for the Zener diode) using KVL:

$$V = R_{thev} \cdot I + V_{thev} \qquad (1 - 35)$$

Solving for I

$$I = -\frac{1}{R_{thev}} \cdot V + \frac{V_{thev}}{R_{thev}} \qquad (1 - 36)$$

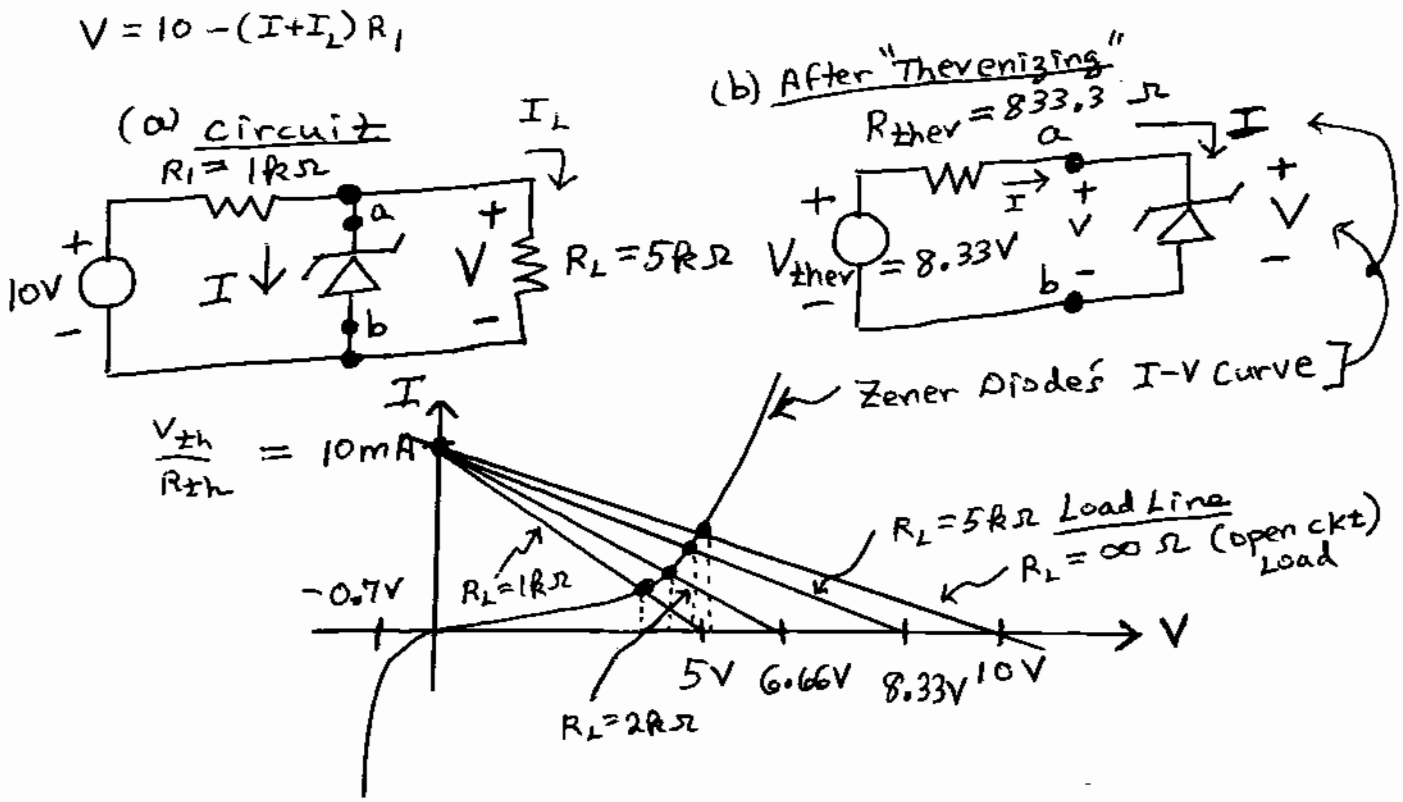
This externally imposed I-V curve plots as a straight line of the form y = mx + b, where I plays the role of y, and V plays the role of x. Recall that m is the slope, and b is the y-intercept. This I-V curve may be plotted (as a load line) on the same set of axes as the Zener diode's I-V curve. It is easily plotted if we note from (1-36) that it has a slope m = $-1/R_{thev}$ and an I-intercept b = V_{thev}/R_{thev} = 10 mA. Also, from (1-35), it is seen that the V intercept is V_{thev}. Note that both I-V curves have to be simultaneously be satisfied, therefore the intersection of the two curves indicates the Zener diode's "operating point", or its voltage and current. We see that the Zener voltage is about 4.9 V. If the load impedance changes from R_L = 5kΩ to R_L = 2kΩ, (thereby dramatically increasing the load current) now the new load line can be calculated:

$$V_{thev} = 10 \cdot \frac{2}{2+1} \qquad R_{thev} = \frac{2 \cdot 10^3 \cdot 1 \cdot 10^3}{2 \cdot 10^3 + 1 \cdot 10^3}$$

$$V_{thev} = 6.666667 \quad V \qquad R_{thev} = 666.666667 \quad \Omega$$

The new load line's V intercept is 6.666 V, and its I intercept is 6.66/666 = 10 mA. The load line for R_L = 2kΩ is also plotted in Fig. 1-18. We see that the output voltage has gone down only a very small amount, to about 4.85 V. The voltage regulation circuit seems to work well, as long as the V-intercept value, V_{thev} remains above the 5-volt Zener knee voltage. In similar fashion, the load line for R_L = 1kΩ, is plotted. Now the output voltage is only about 4.5 V. Note that for R_L < 1kΩ, the output voltage will decrease rapidly; the circuit "drops out of regulation" for R_L < 1kΩ.

Fig. 1-18. Zener Diode Voltage Regulation Circuit. (a) Circuit diagram (b) I-V curve of Zener diode with load lines (c) Thevenin equivalent circuit seen from the terminals of the Zener diode.

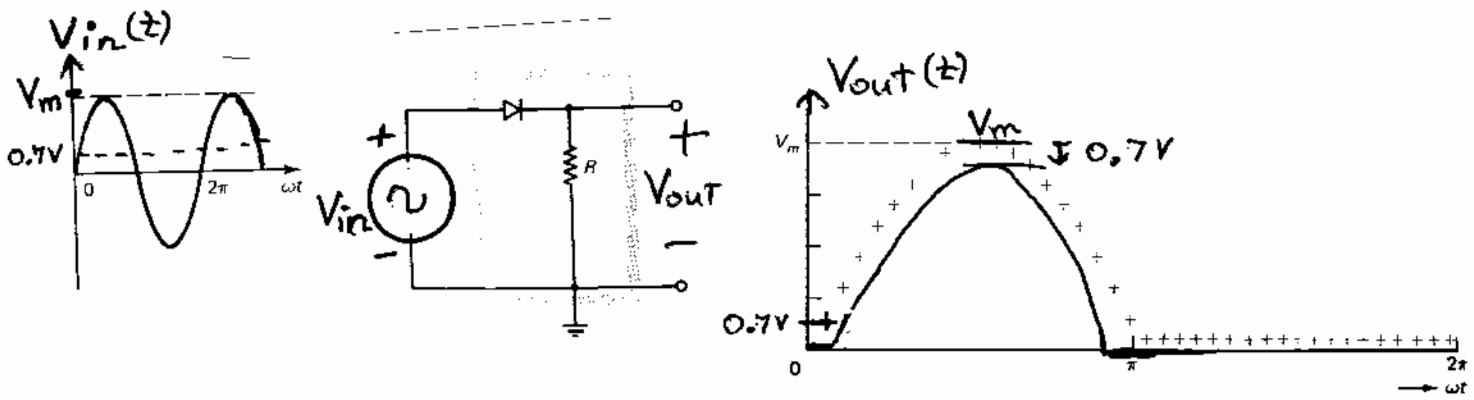


1.8 Diode Rectifier Circuits

1.8.1 Half-wave Diode Rectifier

The diode ***half-wave rectifier*** circuit is shown in Fig. 1-19. Its predicted performance, based upon the ideal diode model of Fig. 1-17(a), is shown as well. During the first (positive) half of the ac input voltage cycle, the diode conducts and the output follows the input. During the second (negative) half the of the ac input voltage cycle, the diode is OFF, and no current flows through the output resistor R, so the output voltage is zero. Note that this circuit effectively "chops off the negative half" of an ac voltage waveform.

Fig. 1-19. Half Wave Rectifier Circuit (a) Circuit diagram and input waveform (b) Output waveform predicted using the ideal diode model



The ***Fourier series expansion*** of the half-wave rectified waveform is given by

$$v(t) = Vm\left[\left(\frac{1}{\pi} + \frac{1}{2}\cdot\sin(\omega\cdot t) - \frac{2}{3\cdot\pi}\cdot\cos(2\cdot\omega\cdot t) - \frac{2}{15\cdot\pi}\cdot\cos(4\cdot\omega\cdot t)\right) + \ldots\right] \qquad (1 - 37)$$

$= (V_m - 0.7V)$

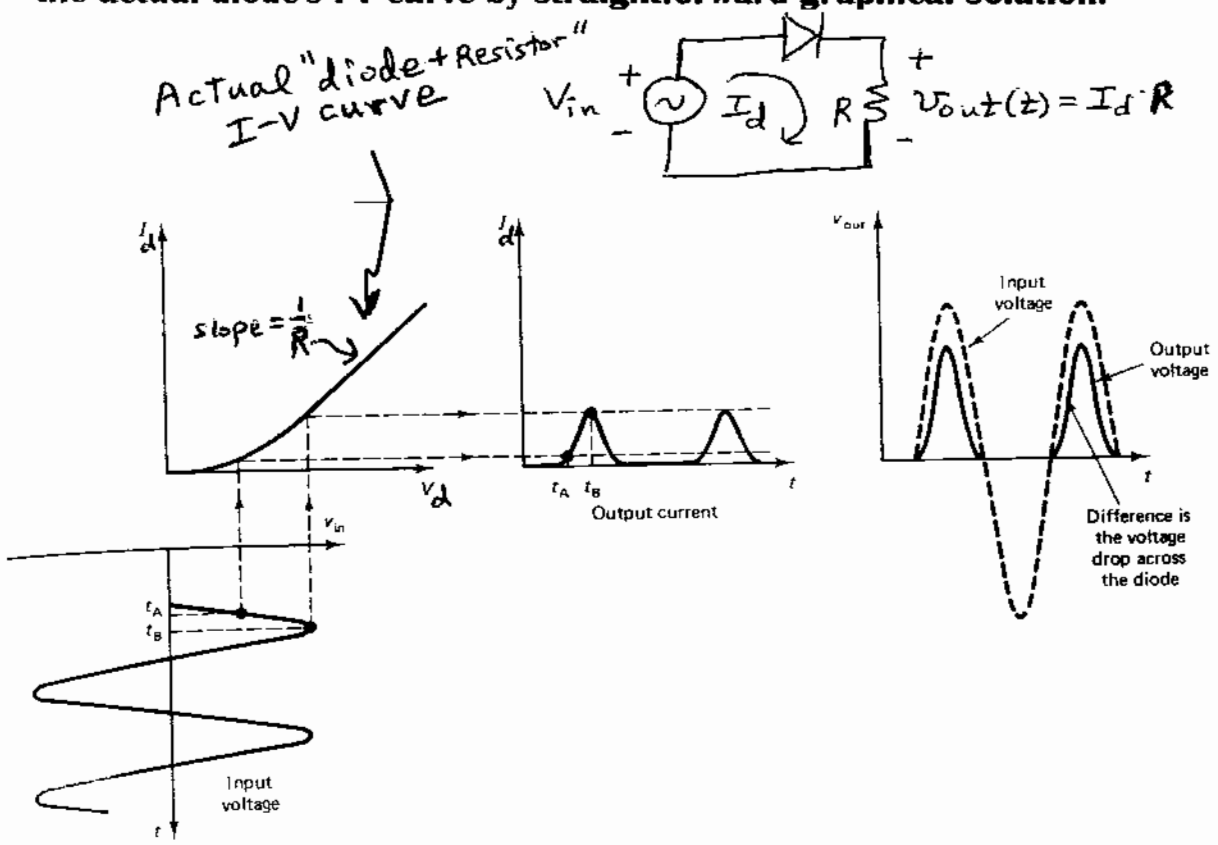
(if diode's cut in voltage, or "forward voltage drop" taken into account)

Note the strongest sinusoidal component (the ***fundamental*** component) has the frequency of the source (ω), and the frequency of the other sinusoidal (***even harmonic***) components successively doubles, while their amplitude rapidly tapers off, so the series rapidly converges.. Note that an analog dc meter would read the average (dc) value of Vm/π volts.

A more realistic graphical prediction of the rectifier's performance is based upon the diode's true I-V curve. This appears in Fig. 1-20. Each point in the input signal is "reflected off of" the diode's I-V curve to plot the output current. Next this output current is multiplied by the value R to convert it into a plot of output current. Note that the predicted output does not quite follow the positive input voltage (it is somewhat below this value), and the output does not rise above zero at the instant the input waveform rises above zero volts. This is due to the varying voltage drop across the diode. Nevertheless, the ideal diode model does a good job of roughly predicting the operation of the circuit.

The use of the diode model in Fig. 1-17(b), involving the 0.7 V threshold with zero output resistance, would give accuracy that is intermediate between the two approaches described above. With this model, the output voltage waveform would start rising above zero when the input rises above 0.7 V, and the output would reach a maximum value that is 0.7 V below the maximum input value. Of course this 0.7 V drop contributes to energy loss and diode heating. In a high current application, the diode may have to be "heat sunk". Schottky diodes are used to decrease this loss, since they have a junction drop of only 0.3 V, although they are more expensive.

Fig. 1-20. Finding the output voltage of a half-wave rectifier using the actual diode's I-V curve by straightforward graphical solution.

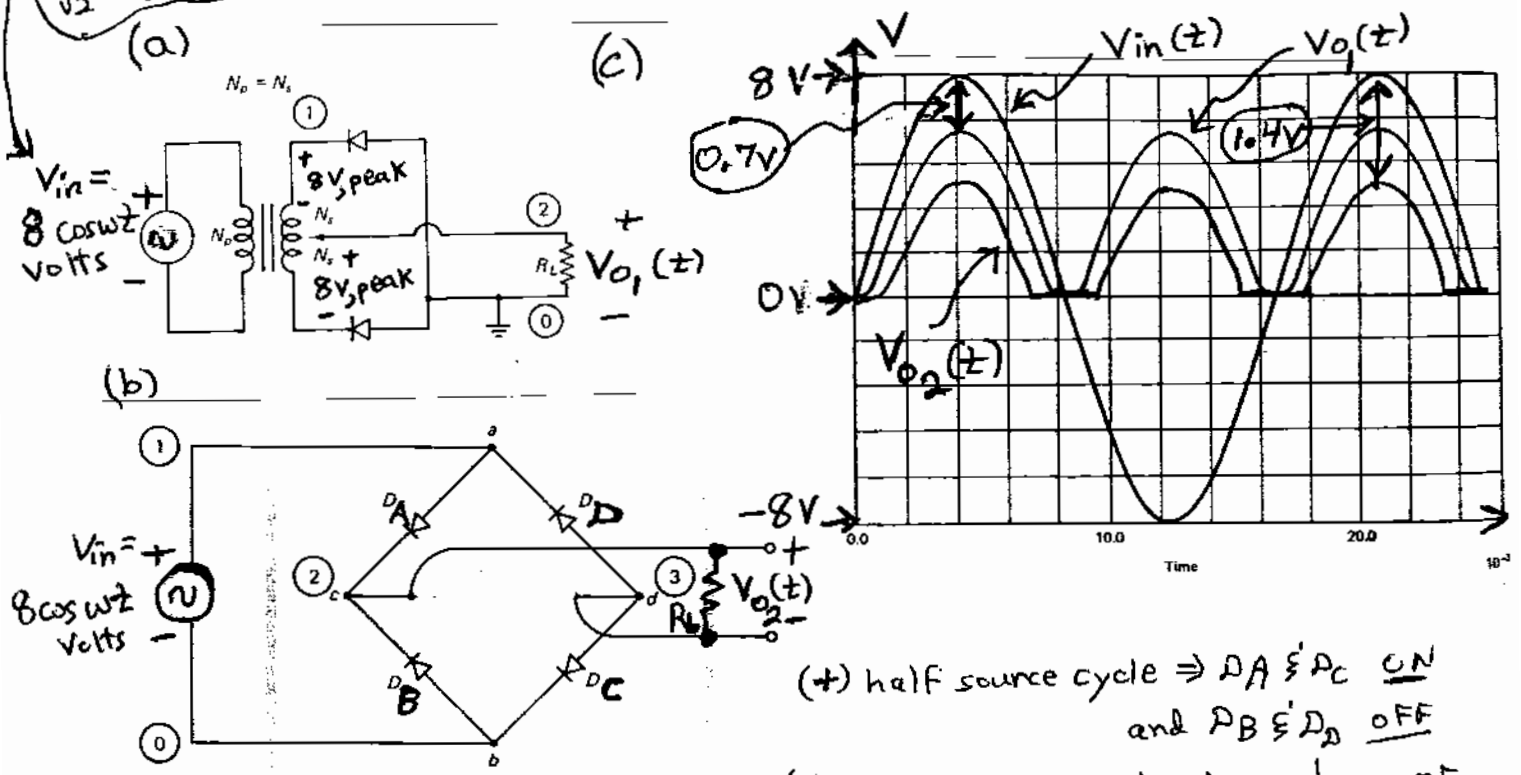


1.8.2 Full-Wave Diode Rectifier

A ***full-wave diode rectifier*** is made with either two diodes and a center-tapped transformer (Fig. 1-21(a)), or with four diodes connected in a "bridge" configuration (Fig. 1-21(b)). The resulting output voltage waveforms developed across load resistor RL for circuits (a) or (b), assuming the 0.7 V threshold diode model of Fig 1-17(b), is shown in Fig 1-21(c). Note that the full-wave recifier is roughly an "***absolute value***" calculating circuit.

"8 V_{peak} OR $\frac{8}{\sqrt{2}}$ V_{rms}"

Fig. 1-21. Full-Wave Diode Rectifier. (a) Two-diode circuit (b) Four-diode bridge (c) Example input and output voltage waveforms based on 0.7 V threshold diode model.



(+) half source cycle ⇒ D_A & D_C ON and D_B & D_D OFF

(−) half source cycle ⇒ D_A & D_C OFF and D_B & D_D ON

PIV = peak rev. bias voltage that can be withstood by diode before it breaks down.
aka inverse voltage

Circuit (a) operates as follows: During positive halves of the cycle, the top terminal of the secondary winding is positive with respect to the grounded center tap, while the bottom terminal is negative. Thus the top diode is ON and the bottom diode is OFF. Therefore the output voltage directly *follows* the positive half of the input waveform *minus* one 0.7 V junction drop. During negative halves of the cycle, the situation is reversed, and the bottom diode is ON while the top diode is OFF. Now the output voltage follows the *inverted* negative half of the input waveform minus one 0.7 V junction drop.

Circuit (b) operates as follows: During positive halves of the cycle, diodes A and C are ON while B and D are OFF, therefore the output voltage follows the positive half of the input waveform *minus* two junction drops (1.4 V). During the negative halves of the cycle, the situation is reversed; diodes B and D are ON while A and C are OFF. Therefore, the output voltage follows the inverted negative half of the input waveform minus two junction drops (1.4 V). Note that the 4-diode bridge circuit has the advantage of not requiring a center-tapped transformer, but the disadvantage of doubled voltage drop and increased energy loss (and heating) in the rectifying diodes.

Ignoring the junction drops, the ideal full-wave rectified waveform has the following Fourier series expansion:

$$v(t) = Vm \cdot \left(\frac{2}{\pi} - \frac{4}{3 \cdot \pi} \cdot \cos(2 \cdot \omega \cdot t) - \frac{4}{15 \cdot \pi} \cdot \cos(4 \cdot \omega \cdot t) + \ldots \right) \qquad (1 - 38)$$

(More accurate) → $(V_m - 0.7)$

Note that the fundamental frequency component is now at ***twice*** the frequency of the source, and that once again, only even harmonics are present. Now the dc (average value) term is twice that of the half-wave rectified wave.

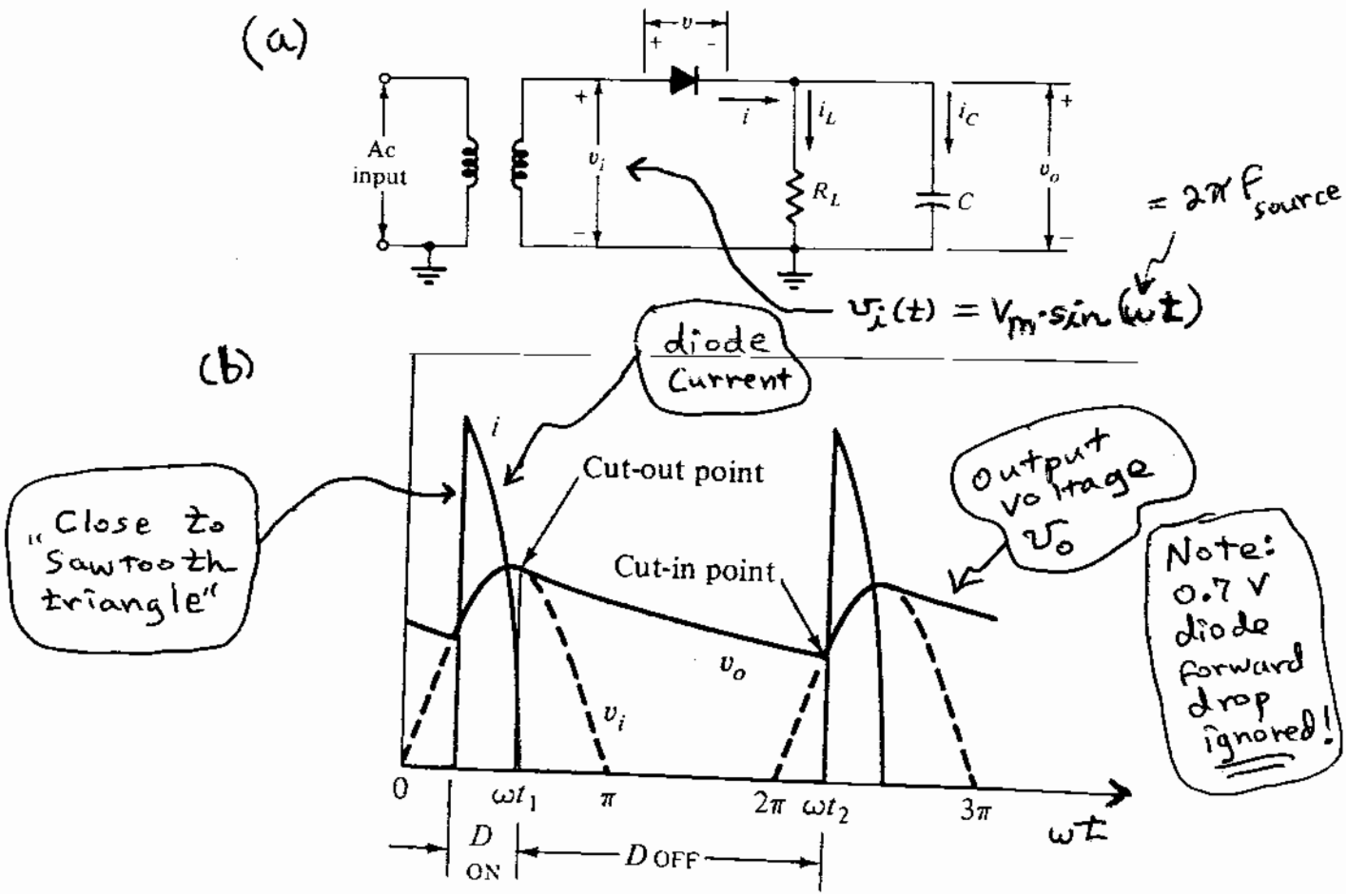
1.8.3 Diode Peak Detector: Rectifier with capacitor filter

The diode ***peak detector***, or ***dc power supply circuit*** is a diode rectifier (either half or full-wave) followed by a capacitor (C) placed in parallel with the load resistor (R_L).

Fig. 1-22 shows the circuit and output voltage and diode current waveforms for a half-wave rectifier followed by a capacitor filter. The capacitor will charge up to the the peak value of the output waveform (***Vm***).

As the input source voltage on the left side of the diode drops below ***Vm***, the capacitor holds the voltage value of Vm volts on the right side of the diode, therefore the diode turns OFF. The voltage across the capacitor, which is also the output voltage, ***Vo(t)***, begins to "droop" as it discharges through the load resistor R_L. Assuming that C has been chosen so that the time constant $C*R_L$ is considerably longer than the period of the half-wave rectified waveform (T = ***1/fsource***), the output voltage droop will not be large before the next "hump" in the waveform comes along. When the input voltage rises above the gradually drooping value of ***Vo***, the diode turns on, and diode charging current (***I***) flows. (See Fig. 1-22(b).) Thus the output voltage consists of a large dc component that is only slightly below Vm volts, along with a (usually small) "***sawtooth ac ripple***" waveform with a period of (***1/fsource***) Hertz.

Fig. 1-22. Peak Detector: Half wave rectifier with a capacitor filter. (a) circuit (b) output voltage and diode current waveforms



A full-wave rectifier followed by a capacitor filter is shown in Fig. 1-23. Note that for a given capacitor C, the output of the full-wave bridge contains about half as much ripple. The magnitude of the ripple voltage, Vr, can be approximately predicted by approximating the ripple voltage wave by a piecwise linear (triangular) waveform. An upward sloping line can approximate the charging interval labelled ωT_1 and a downward sloping line can approximate the discharge interval labelled ωT_2. The average value of the output voltage is

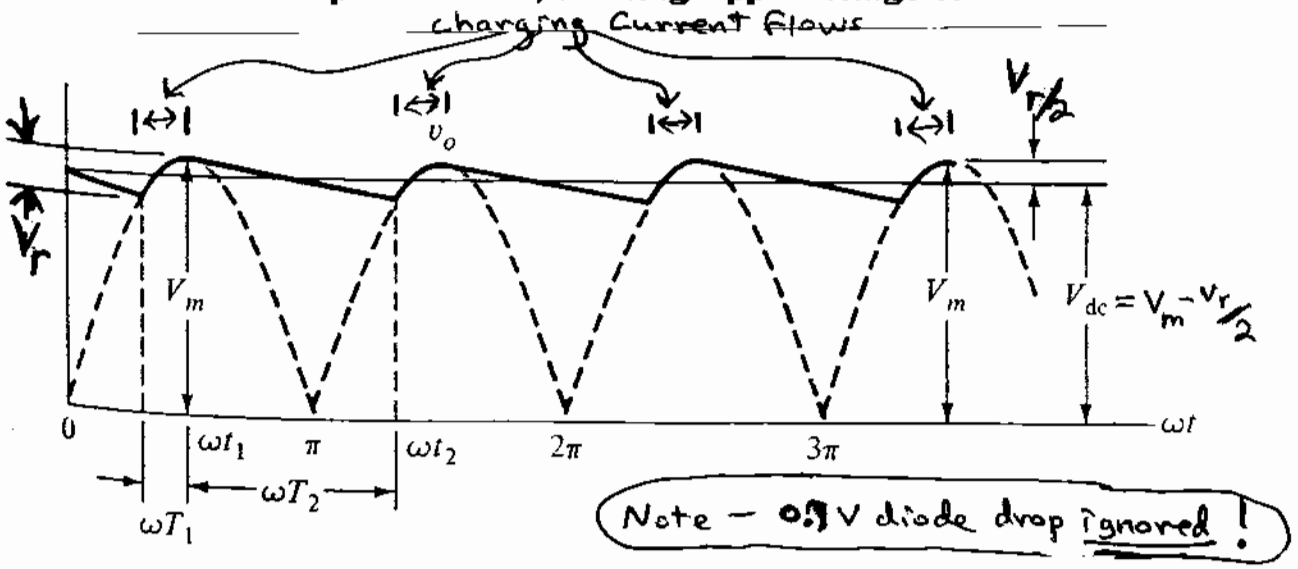
dc voltage across Load Resistance R_L

$$V_{dc} \cong V_m - \frac{V_r}{2} \cong V_m \quad \text{(For reasonably small } V_r \text{ (ripple voltage))}$$

dc current through R_L

$$I_{dc} \cong \frac{V_{dc}}{R_L} \qquad (1-39)$$

Fig. 1-23. Approximate load voltage waveform for a full-wave rectifier with a capacitor filter, showing ripple voltage Vr



To approximately express ***Vr*** as a function of load curernt and capacitance, note that time T_2 represents the total nonconducting time for the diode. The capacitor is assumed to be steadily discharging at a constant rate of ***Idc.*** Therefore, the capacitor will lose an amount of charge equal to ***Idc*T$_2$*** during this interval.

Remember

$$I_{dc} \cong \frac{V_{dc}}{R_L}$$

Therefore the change in capacitor voltage can be found from the defining equation for capacitance:

$$C \triangleq \frac{Q}{V} \quad \Rightarrow \quad V = \frac{Q}{C} \quad \Rightarrow \quad \Delta V = V_r = \frac{\Delta Q}{C} = \frac{I_{dc} \cdot T_2}{C} \qquad (1-40)$$

To get the best possible filter action, a large enough capacitor will be chosen so as to experience only a small amount of droop (***Vr*** is typically only 1 or 2 % of the total dc output voltage). Therefore we see that the charging time T_1 will be very small compared to the discharging time T_2. Therefore T_2 will approach the duration of a half of a cycle. Therefore

$$T_2 \approx \frac{T_{source}}{2} = \frac{1}{2 \cdot f_{source}} \qquad \text{(For full-wave rectifier)}$$

and from (1-40), the ripple voltage amplitude is approximately

$$V_r = \frac{I_{dc}}{2 \cdot f_{source} \cdot C} \qquad \text{(For full-wave rectifier)} \qquad (1-41)$$

(where $I_{dc} = \frac{V_{dc}}{R_L}$)

And from (1-39) the dc component at the output is approximately

$$V_{dc} = V_m - \frac{I_{dc}}{4 \cdot f_{source} \cdot C} \approx V_m \qquad (1-42) \qquad \text{(For full-wave rect.)}$$

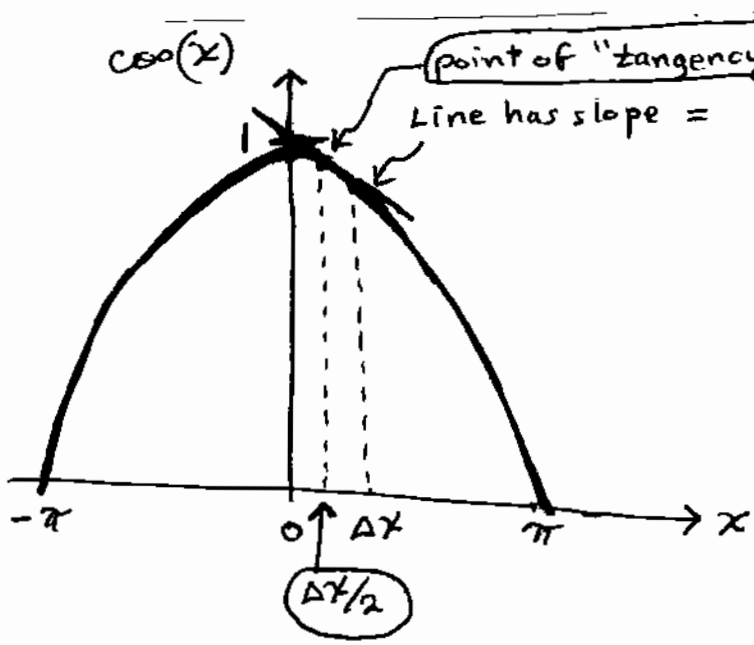
A similar analysis for a half-wave diode rectifier followed by a capacitor filter can be performed, and it should come as no surprise that for this case, the ripple voltage is twice as great for a given value of C: Now $T_2 \cong T_{source} = \frac{1}{f_{source}}$

$$V_r = \frac{I_{dc}}{f_{source} \cdot C} \qquad V_{dc} = V_m - \frac{I_{dc}}{2 \cdot f_{source} \cdot C} \qquad (1-43) \qquad \text{(For Half-wave rect.)}$$

$$\cong V_m$$

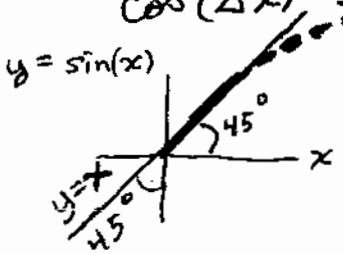
Aside: Develop approximation $\boxed{\cos(\Delta x) \cong 1 - \frac{\Delta x^2}{2}}$ (For $\Delta x \ll 1$)

Proof:



$$\cos(\Delta x) \cong 1 + \left(\frac{d\cos x}{dx}\bigg|_{x=\frac{\Delta x}{2}} \right) \cdot \Delta x$$

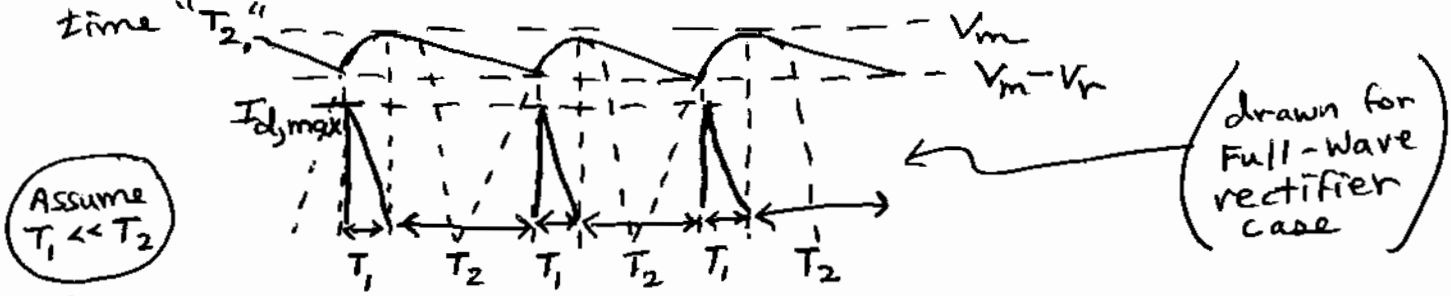
$$\cos(\Delta x) \cong 1 - \underbrace{\sin\left(\frac{\Delta x}{2}\right)}_{\left(\approx \frac{\Delta x}{2} \text{ for } \Delta x \ll 1\right)} \cdot \Delta x = \boxed{1 - \frac{\Delta x^2}{2}}$$



(Ex: sin (0.1 radians) = 0.0998
sin (0.2 radians) = 0.1987
sin (0.5 radians) = 0.479)

(End of Proof)

Consider now the diode current pulses that flow for a brief time "T_1" in order to replenish the charge lost by the capacitor during the much longer discharge time "T_2"



∴ For Full-wave rectifier $T_2 \approx T_{source}/2$; for Half-wave rectifier $T_2 \approx T_{source}$

62-C

Using the small angle approximation for cos(Δx), assuming $\omega_{source} \cdot T_1 << 1$

$$Vm - Vr = Vm \cdot \cos\left(-\omega_{source} \cdot T_1\right) = Vm \cdot \cos\left(\omega_{source} \cdot T_1\right) = Vm\left[1 - \frac{\left(\omega_{source} \cdot T_1\right)^2}{2}\right]$$

Allows us to solve for the short charging time T1:

$$T_1 = \frac{1}{\omega_{source}} \cdot \sqrt{\frac{2 \cdot Vr}{Vm}} = \frac{1}{2 \cdot \pi \cdot f_{source}} \cdot \sqrt{\frac{2 \cdot Vr}{Vm}}$$

But the charge lost during the diode "OFF" time, ΔQlost, due to the capacitor discharging through the load resistor RL can be found in two ways. First, it can be found in terms of the charge removed (at a nearly constant rate) from the capacitor by the load resistor, which is the (nearly constant) average load resistor current times the discharge time "T2".

$$\Delta Q_{lost} = I_{Lavg} \cdot T_2$$

But the average current through the load resistor is approximately Vm/RL, and for the full-wave diode bridge rectifier circuit, T2 is approximately equal to one-half source period, Tsource/2, since the diode conduction time, T1, is considered to be quite short (T1 << T2).

$$\Delta Q_{lost} = \frac{Vm}{R_L} \cdot T_2 = \frac{Vm}{R_L} \cdot \frac{T_{source}}{2} = \frac{Vm}{R_L} \cdot \frac{1}{2 \cdot f_{source}}$$

ΔQlost can alternately be found by finding the area under the (approximately TRIANGULAR) capacitor charging current pulse, which has an amplitude Icmax, and a duration of time T1, since the charge supplied to the capacitor during time period T1 must equal the charge lost through RL during the discharge cycle during time period T2.

$$\Delta Q_{lost} = \frac{1}{2} \cdot base \cdot height = \frac{1}{2} \cdot T_1 \cdot I_{Cmax}$$

Equating these two expressions for ΔQlost yields

$$\frac{Vm}{R_L} \cdot \frac{1}{2 \cdot f_{source}} = \frac{1}{2} \cdot T_1 \cdot I_{Cmax}$$

Substituting the expression found above for T1,

$$\frac{Vm}{R_L} \cdot \frac{1}{2 \cdot f_{source}} = \frac{1}{2} \cdot \left(\frac{1}{2 \cdot \pi \cdot f_{source}} \cdot \sqrt{\frac{2 \cdot Vr}{Vm}}\right) \cdot I_{Cmax}$$

Solving for Icmax yields

$$I_{Cmax} = 2\cdot\pi\cdot\frac{Vm}{R_L}\cdot\sqrt{\frac{Vm}{2\cdot Vr}}$$

During the charging interval T1, the diode current must supply BOTH the capacitor current AND also an approximately constant current Vm/RL through the load resistor. Thus the maximum diode current is

$$I_{Dmax} = I_{RL} + I_{Cmax}$$

$$I_{Dmax} = \frac{Vm}{R_L} + 2\cdot\pi\cdot\frac{Vm}{R_L}\cdot\sqrt{\frac{Vm}{2\cdot Vr}} = \frac{Vm}{R_L}\cdot\left(1 + 2\cdot\pi\cdot\sqrt{\frac{Vm}{2\cdot Vr}}\right)$$

Equation 3.35 in Sedra & Smith Text (Note Vm is "Vp" in the textbook.)

The above equation is an important result, because it permits us to find the PEAK DIODE CURRENT in a full-wave rectifier circuit. This peak diode current is considerably higher than the average diode current, and a power diode used in the full-wave rectifier circuit must be rated to withstand at least this amount of peak current.

In addition, we also want to know the AVERAGE DIODE CURRENT of each diode in a full-wave bridge, since this is another important diode parameter that must be specified when designing a full-wave diode rectifier. Each diode conducts ONLY ONCE PER SOURCE CYCLE (on alternate half cycles), therefore, the average diode current can be found as

$$I_{Davg} = \frac{TOTAL\_CHARGE\_TRANSFERRED\_THROUGH\_DIODE\_PER\_CYCLE}{T_{source}} = \frac{\Delta Q}{T_{source}}$$

The total charge transferred through the diode per cycle is the area under the triangular diode current pulse,

$$\Delta Q = \frac{1}{2}\cdot base\cdot height = \frac{1}{2}\cdot T_1\cdot I_{Dmax} = \frac{1}{2}\cdot T_1\cdot\left[\frac{Vm}{R_L}\cdot\left(1 + 2\cdot\pi\cdot\sqrt{\frac{Vm}{2\cdot Vr}}\right)\right]$$

$$I_{Davg} = \frac{\frac{1}{2}\cdot T_1\cdot\left[\frac{Vm}{R_L}\cdot\left(1 + 2\cdot\pi\cdot\sqrt{\frac{Vm}{2\cdot Vr}}\right)\right]}{T_{source}} = \frac{\frac{1}{2}\cdot\left(\frac{1}{2\cdot\pi\cdot f_{source}}\cdot\sqrt{\frac{2\cdot Vr}{Vm}}\right)\cdot\left[\frac{Vm}{R_L}\cdot\left(1 + 2\cdot\pi\cdot\sqrt{\frac{Vm}{2\cdot Vr}}\right)\right]}{\left(\frac{1}{f_{source}}\right)}$$

62-E

$$I_{Davg} = \frac{\frac{1}{2}\cdot\left(\frac{1}{2\cdot\pi\cdot f_{source}}\cdot\sqrt{\frac{2\cdot Vr}{Vm}}\right)\cdot\left[\frac{Vm}{R_L}\cdot\left(1+2\cdot\pi\cdot\sqrt{\frac{Vm}{2\cdot Vr}}\right)\right]}{\left(\frac{1}{f_{source}}\right)}$$

Simplifying

$$I_{Davg} = \frac{1}{2\cdot\pi}\cdot\sqrt{\frac{Vr}{2\cdot Vm}}\cdot\frac{Vm}{R_L}\cdot\left(1+\pi\cdot\sqrt{\frac{2\cdot Vm}{Vr}}\right)$$

This equation is NOT in the Sedra & Smith textbook. The textbook's "Idav" expression is only for the average diode current during the charging interval, which is not useful.

Example: Consider a full-wave bridge rectifier that operates directly from the ac power line with

$$Vs(t) = 120\sqrt{2}\cdot\sin(2\cdot\pi\cdot 60\cdot t)\ \text{Volts} \qquad R_L := 300\cdot\Omega \ \text{and} \qquad C := 1000\cdot\mu F$$

Find the approximate ripple voltage, the PIV rating of the diodes, the peak diode current, and the average diode current, the average load current, and the average power delivered to the load.

SOLUTION:

$$V_{dc} = 120\cdot\sqrt{2}\cdot V - 2\cdot(0.7\cdot V) - \frac{Vr}{2} \qquad Vr = \frac{\left(\frac{Vdc}{R_L}\right)}{2\cdot f_{source}\cdot C} = \frac{\left[120\cdot\sqrt{2}\cdot V - 2\cdot(0.7\cdot V) - \frac{Vr}{2}\right]}{R_L\cdot 2\cdot 60\cdot Hz\cdot C}$$

Solving for Vr

$$Vr := 336.61125496954281171\cdot\frac{V}{(240.\cdot R_L\cdot Hz\cdot C + 1.)} \qquad \boxed{Vr = 4.611\ V}$$

$$V_{dc} := 120\cdot\sqrt{2}\cdot V - 2\cdot(0.7\cdot V) - \frac{Vr}{2} \qquad V_{dc} = 166\ V$$

$$Vm := 120\cdot\sqrt{2}\cdot V - 2\cdot(0.7\cdot V) \qquad Vm = 168.306\ V$$

$$PIV := 120\cdot\sqrt{2}\ V - 0.7V \qquad \boxed{PIV = 169.006\ V}$$

$$I_{Davg} := \frac{1}{2\cdot\pi}\cdot\sqrt{\frac{Vr}{2\cdot Vm}}\cdot\frac{Vm}{R_L}\cdot\left(1+\pi\cdot\sqrt{\frac{2\cdot Vm}{Vr}}\right) \qquad \boxed{I_{Davg} = 0.291\ A}$$

$$I_{Dmax} := \frac{Vm}{R_L}\cdot\left(1+2\cdot\pi\cdot\sqrt{\frac{Vm}{2\cdot Vr}}\right) \qquad \boxed{I_{Dmax} = 15.62\ A}$$

Note that the diode charging current peaks are suprisingly large!

$$I_{RLavg} := \frac{V_{dc}}{R_L} \qquad \boxed{I_{RLavg} = 0.553\ A} \qquad Pavg := V_{dc}\cdot I_{RLavg} \qquad \boxed{Pavg = 91.853\ W}$$

Besides its widespread use in performing ac-dc conversion in power supply circuits, the diode peak detector circuit is also commonly used as a an "***envelope detector***" (or demodulator) in AM radio receivers.

An AM (amplitude-modulated) radio wave consists of a radio-frequency "**carrier wave**" (say, a 1-MHz sine wave) whose amplitude has been modulated (varied) at a (much slower) audio rate. While theoretically, an alternating current of any frequency flowing through a wire will radiate an electromagnetic (radio) wave. The wire (broadcasting antenna) must be on the order of one-half wavelength in in length for it to radiate it efficiently. Therefore, a "base-band audio" signal (300 - 5000 Hz) ***cannot*** be efficiently radiated by an antenna, since for the low frequencies (300 Hz) the antenna would have to be one-half wavelength long, which would be

$$L_{ant\_300} = \frac{\lambda}{2} = \frac{1}{2}\cdot\frac{c}{f_{low}} = \frac{3\cdot 10^8}{2\cdot 300} = 5\cdot 10^5 \text{ meters} = 313 \text{ miles!}$$

(This antenna length is impractically long!)

Besides the obvious problem with antenna length, there is another practical problem: for the higher audio frequencies (5000 Hz) to be radiated a completely different antenna length is needed:

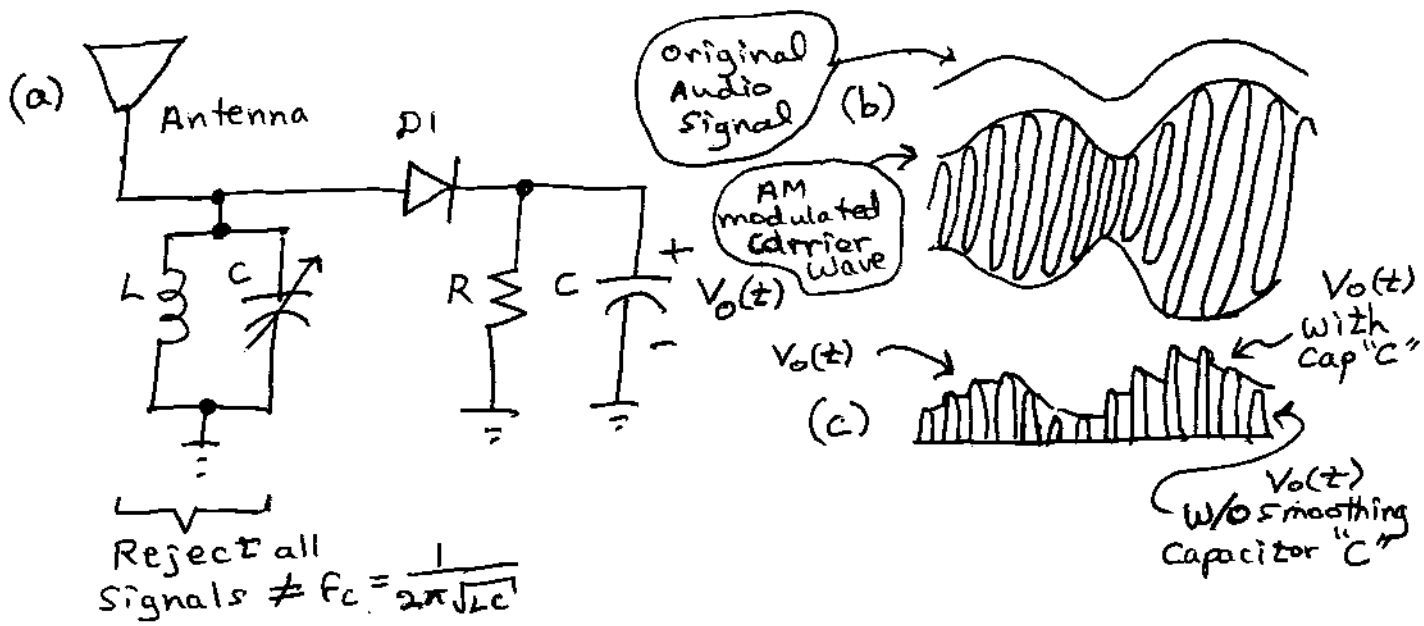
$$L_{ant\_5000} = \frac{\lambda}{2} = \frac{1}{2}\cdot\frac{c}{f_{low}} = \frac{3\cdot 10^8}{2\cdot 5000} = 3\cdot 10^4 \text{ meters} = 19 \text{ miles!}$$

These two practical problems are what motivate us to make the desired audio signal "ride on the back" of the much higher frequency "carrier wave", by gradually varying the amplitude of the carrier wave. For a 1-MHz carrier wave, the antenna only needs to be one length, and it is a much shorter, more practical length!

$$L_{ant\_1000000} = \frac{\lambda}{2} = \frac{1}{2}\cdot\frac{c}{f_{low}} = \frac{3\cdot 10^8}{2\cdot 10^6} = 150 \text{ meters}$$

Another wire suspended in the air, perhaps miles away from the transmitting antenna, will pick up (receive) a greatly attenuated version of the transmitted 1-MHz amplitude-modulated carrier wave (along with any other radio waves that might be present at other carrier frequencies). The circuit of a simple, yet workable, AM radio receiver is shown in Fig. 1-24(a) The other radio frequencies are rejected in the parallel-tuned LC "tank circuit" which has been tuned to resonate at the desired carrier frequency (1 MHz) and thus exhibits infinite impedance at this frequency, and a low impedance at all others. Thus received carrier waves at all other frequencies except the desired one (1 MHz) are shunted to ground. Only the 1-MHz AM-modulated wave remains. The AM modulated carrier wave is shown in Fig. 1-24(b). The demodulated audio signal that appears at the output of the peak detector, which rode on the "amplitude" of the carrier wave, is shown in Fig. 1-24(c). Note that the RC time constant must be chosen to be considerably longer than the carrier frequency period, 1/fcarrier, in order to minimize the droop between carrier wave voltage peaks. At the same time, however, the RC time constant must be chosen to be considerably shorter than the highest audio frequency of interest 1/faudio_high, so that the peak detector (now better called an "***envelope detector***") can accurately follow the variations in the detected audio waveform.

Fig. 1-24. Simple AM Radio Receiver (a) Circuit (b) AM modulated wave (c) Output of diode peak detector circuit



Use of Low-pass Filter to Reduce Voltage Ripple, Vr

Returning to the dc power supply application, it should be mentioned that low-pass RC or LC filter sections (such as those shown in Fig. 1-25) can be used to provide lower ripple voltage, ***Vr***. The the break frequency of the low-pass filter is placed well below the frequency of the fundamental sinusoid, which for a full-wave rectifier is $\mathbf{2*f_{source}}$ and for a half-wave rectifier is $\mathbf{f_{source}}$. If the break frequency is placed too close to dc, the required capacitor value will be large, and thus it will be too expensive, and the turn on transient (voltage ramp-up time) will be too long. If the break frequency is chosen to be too high, on the other hand (but still below the fundamental frequency), too much of the fundamental frequency will get through and contribute to ripple voltage, since no low-pass filter exhibits an ideal "brick wall" frequency response characteristic. With an ideal low-pass filter at the output, only the dc (average value) component will be passed. We have found from (1-38) that for a full-wave rectifier the dc value will be substantially lower than for the capacitor filter. It will be reduced to

$$Vdc = \frac{2 \cdot Vm}{\pi} \qquad (1 - 43)$$

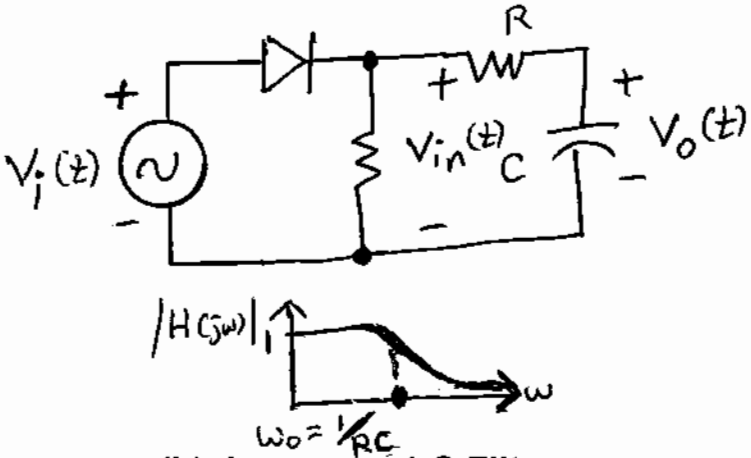
For a half-wave rectifier, the dc output voltage will be reduced again by half, since the average value of the half-wave rectified voltage is only one-half that of the full-wave rectified waveform. From (1-37) we find that

$$Vdc = \frac{Vm}{\pi} \qquad (1 - 44)$$

If a capacitor filter is followed by an LC (or RC) lowpass filter, we have a "capacitive input filter" (Fig. 1-25(d), then the output voltage will be much closer to the peak value, Vm. The LC low-pass filter section that follows the capacitor filter simply serves to filter out the ripple component present in voltage developed across the capacitor.

Fig. 1-25. Use of More Complex Low-pass Filter Sections to Reduce Ripple (a) 1st-Order RC LPF Section (c) 2nd-order LC filter (d) Capacitive-input Filter

(a) Low-pass RC Filter

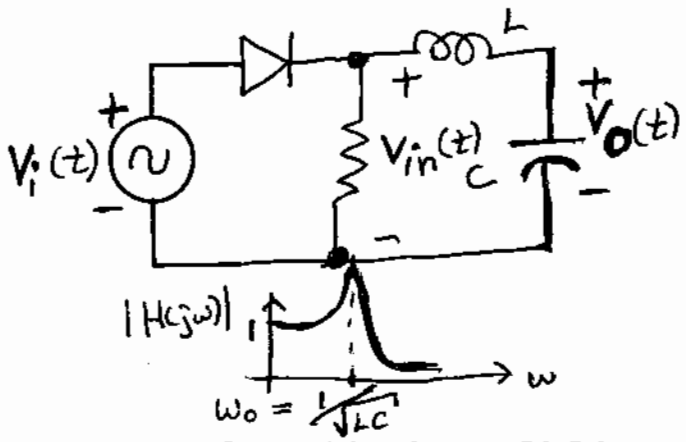


Transfer Function

$$|H(j\cdot\omega)| = \left| \frac{\frac{1}{j\cdot\omega\cdot C}}{R + \frac{1}{j\cdot\omega\cdot C}} \right|$$

$$|H(j\cdot\omega)| = \frac{1}{\sqrt{(\omega\cdot R\cdot C)^2 + 1}}$$

(b) Low-pass LC Filter

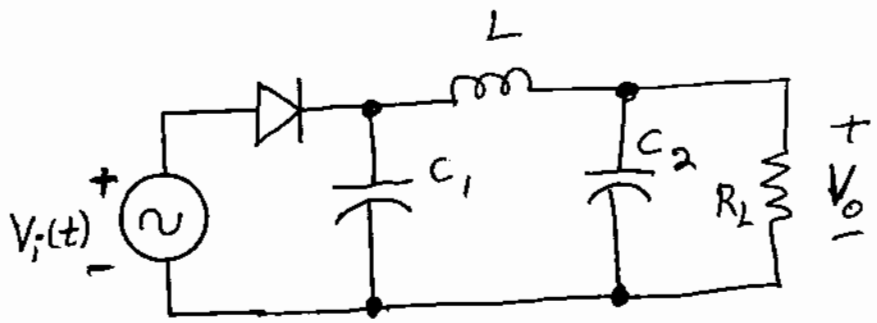


Transfer Function

$$|H(j\cdot\omega)| = \left| \frac{\frac{1}{j\cdot\omega\cdot C}}{j\cdot\omega\cdot L + \frac{1}{j\cdot\omega\cdot C}} \right|$$

$$|H(j\cdot\omega)| = \frac{1}{\left(\omega^2\cdot L\cdot C - 1\right)}$$

(c) Capacitive Input *CLC* low-pass Filter



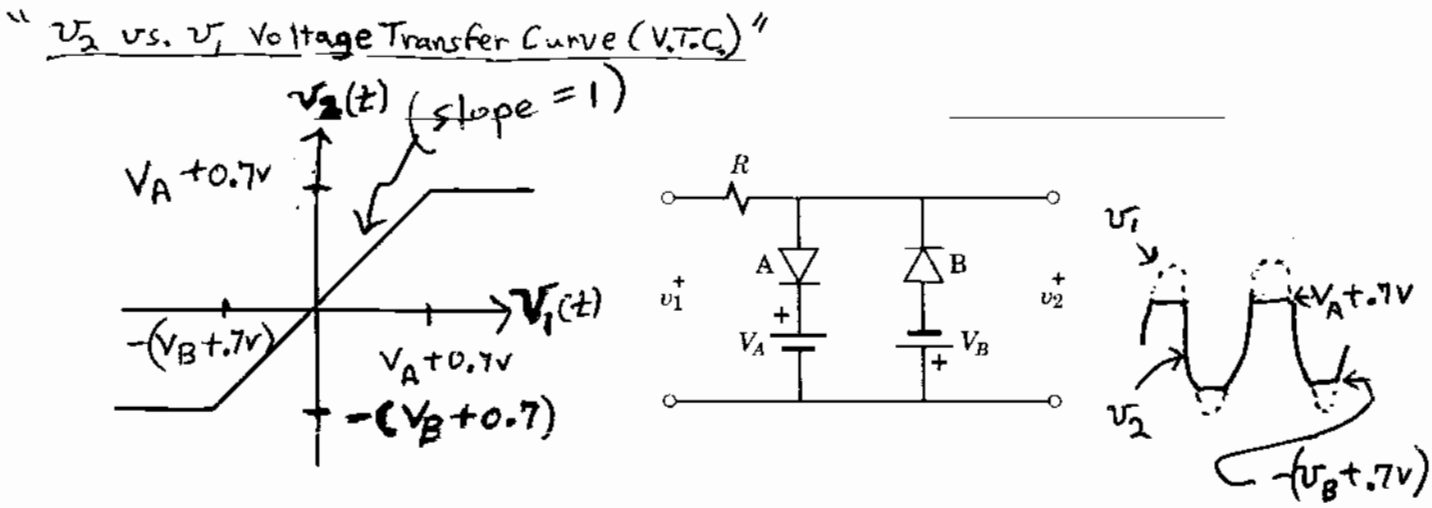
1.9 Diode Voltage Clipper

Fig. 1-26 shows a **voltage clipping circuit** along with its ***Vout vs. Vin voltage transfer curve***. Using the 0.7 V threshold model of Fig. 1-17(b), it is clear that as long as input voltage waveform ***Vin(t)*** remains between $-(V_B+0.7)$ and $+(V_A+0.7)$ volts, neither diode will turn on, and ***Vout = Vin***. But as ***Vin(t)*** drops below the negative limit of $-(V_B+0.7)$ volts, Diode B comes on, and ***Vout*** is held (or clipped) to $-(V_B+0.7)$ volts. Likewise, if Vin(t) rises above the positive limit of $(V_A+0.7)$ volts, Diode A comes on, and ***Vout*** is held (or clipped) to $+(V_A+0.7)$ volts.

If only a positive clipping threshold is desired, Diode B and source V_B can be omitted. Likewise, if only a negative clipping threshold is desired, Diode A and source V_A can be omitted. If we desire a clipping level between -0.7 and +0.7 V, the two voltage sources can be omitted.

Diode clippers are very useful in restricting the range of input signals in devices to protect them from overload. For example, clipping circuits are often inserted in guitar amplifiers to protect the loudspeaker from damage in the event of an over-enthusiastic player (like Ted Nugent!) turns up his instrument too loud. With the clippers in place, if the guitar is turned up too loud, the guitar sound will become distorted (clipped), but the speakers will be spared! Diode clippers are also intentionally used to produce various distortion effects in guitar "distortion pedals".

Fig. 1-26. Diode Clipper and Voltage Transfer Curve



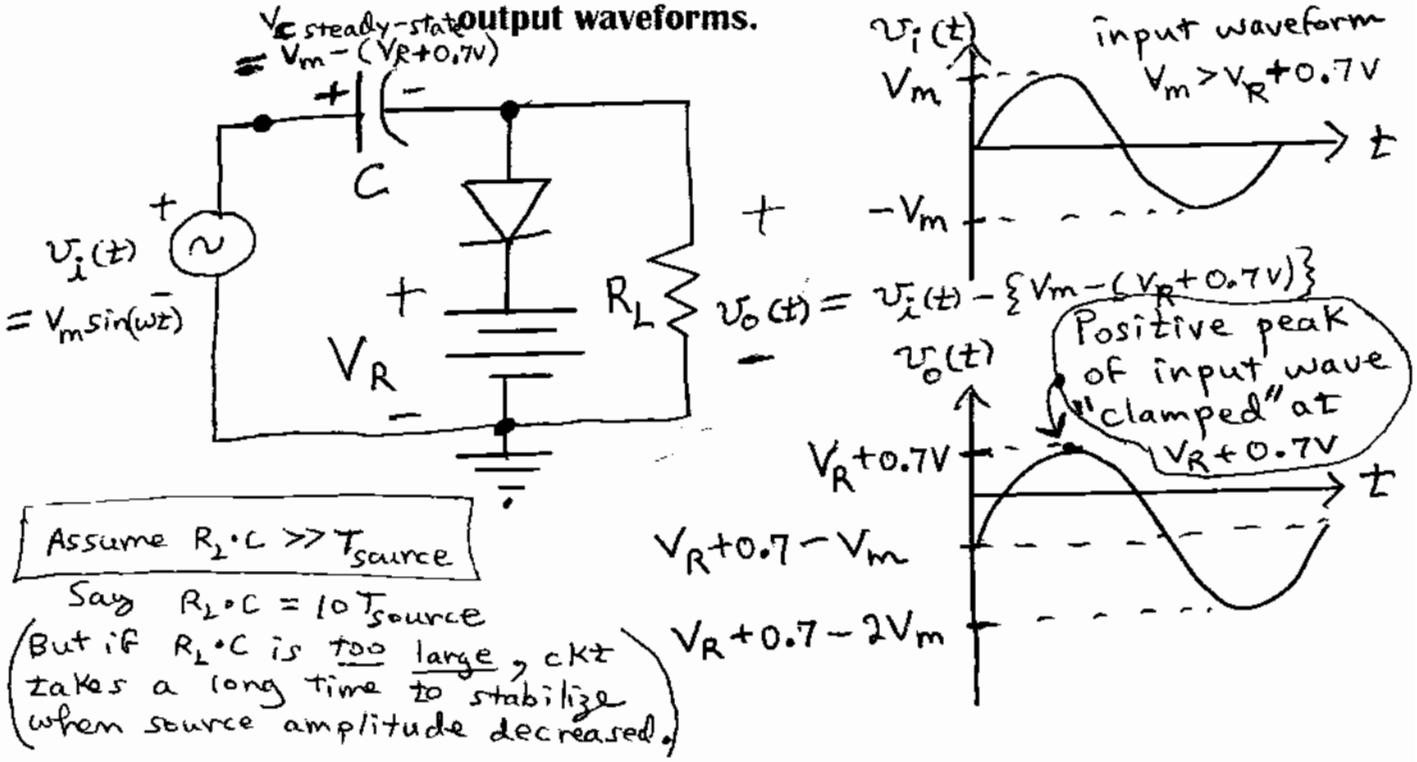
1.10 Diode Voltage Clamper

Fig. 1-27 shows the ***diode clamping circuit*** along with an example input and output voltage waveform. This circuit is used to fix the peak value of a periodic waveform to some predetermined reference voltage, ***(V_R + 0.7)*** volts, which must be ***less*** than the peak value of the ***Vin(t)*** input waveform, ***Vm***. The ***R_L*C*** time constant must be long compared to the period of the input voltage waveform, ***Vs(t)***, so that the capacitor will not discharge appreciably during one cycle.

Assuming that the capacitor is initially uncharged, we see that as the input rises above ***(V_R + 0.7)*** volts, continuing on up to the positive peak of the input voltage waveform ***Vs(t)***, which we shall call ***Vm***, the diode turns ON, allowing the capacitor to charge to ***Vm - (V_R + 0.7)*** volts.

Then, as ***Vs(t)*** drops below its peak value Vm, the diode turns OFF (just as happens in the half-wave rectifier circuit). On a later cycle, the diode will turn on only for the short time needed to charge the capacitor back up to ***Vm - (V_R + 0.7)***, assuming that it loses only a small amount of charge through the load resistor ***R_L*** between cycles. Thus the output voltage waveform, Vo(t), has been shifted so it peaks at ***Vm - [Vm - (V_R + 0.7)] = (V_R + 0.7)*** volts.

Fig. 1-27. Diode clamper circuit with example input and output waveforms.



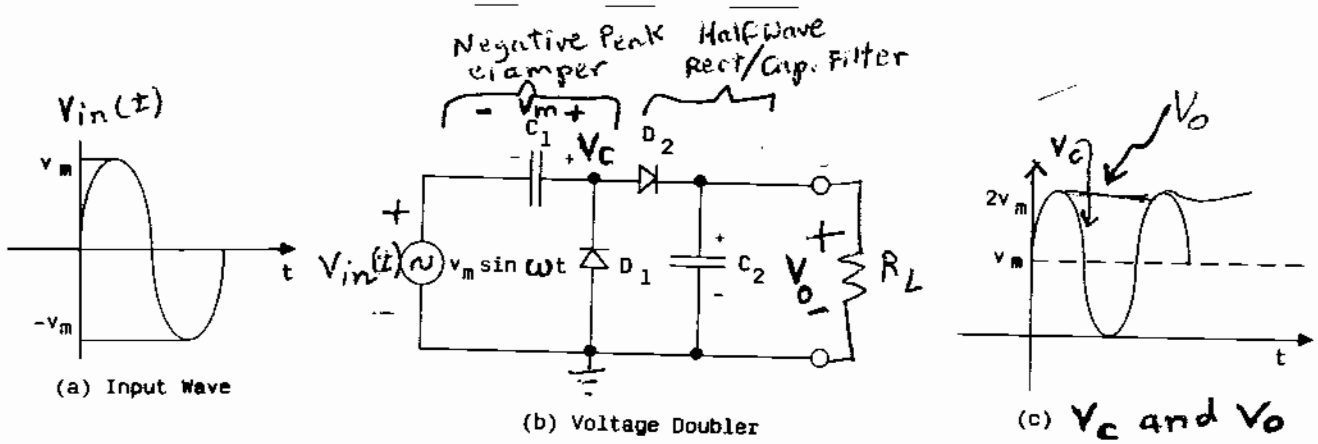
The clamping circuit (or ***dc restoration circuit***) is used in a television receiver to restore the the proper dc offset to a received video signal, so that the peak value of the video ***luminance*** (brightness) signal corresponds to a predetermined "***white reference level***". Signals of lesser amplitude will then correspond to darker light intensities. This is necessary since only the ac component of this television picture signal is detected and amplified, and hence the proper reference level has to be re-established.

Signals can also be clamped such that their negative peak is fixed at a predetermined reference level by reversing the polarity of the diode and the voltage source V_R in Fig. 1-27.

1.10 Voltage Doubler

A voltage doubler ac-to-dc conversion circuit that is widely used in power supply designs is shown in Fig. 1-28. It consists of a ***negative-peak voltage clamper*** circuit (formed by C1 and D1). Note that the sinusoidal input waveform (of amplitude ***Vm***) has its negative peak value (***-Vm***) clamped to 0 V. Thus, the voltage waveform across diode D1 (***Vc***) is a dc-offset version of the input waveform, with a dc value of ***Vm*** volts, alternating between 0 and ***2*Vm***. This ***Vc(t)*** waveform is then presented to the input of a ***half-wave rectifier/capacitor filter*** circuit (formed by D2 and C2). Initially the diode conducts, allowing the capacitor to charge up to the peak value (***2*Vm - 0.7***) volts. Then, as Vc drops below (***2*Vm - 0.7***) volts, the diode turns OFF. Thus the output voltage developed across C2 is held at an approximate dc value of (***2*Vm - 0.7***) volts. Note that the input sinusoidal waveform Vin(t) has been effectively doubled!

Fig. 1-28. Voltage doubler ac-to-dc conversion circuit with example waveforms. This circuit can be thought of as a negative peak voltage clamper followed by a half-wave rectifier/capacitive filter circuit.

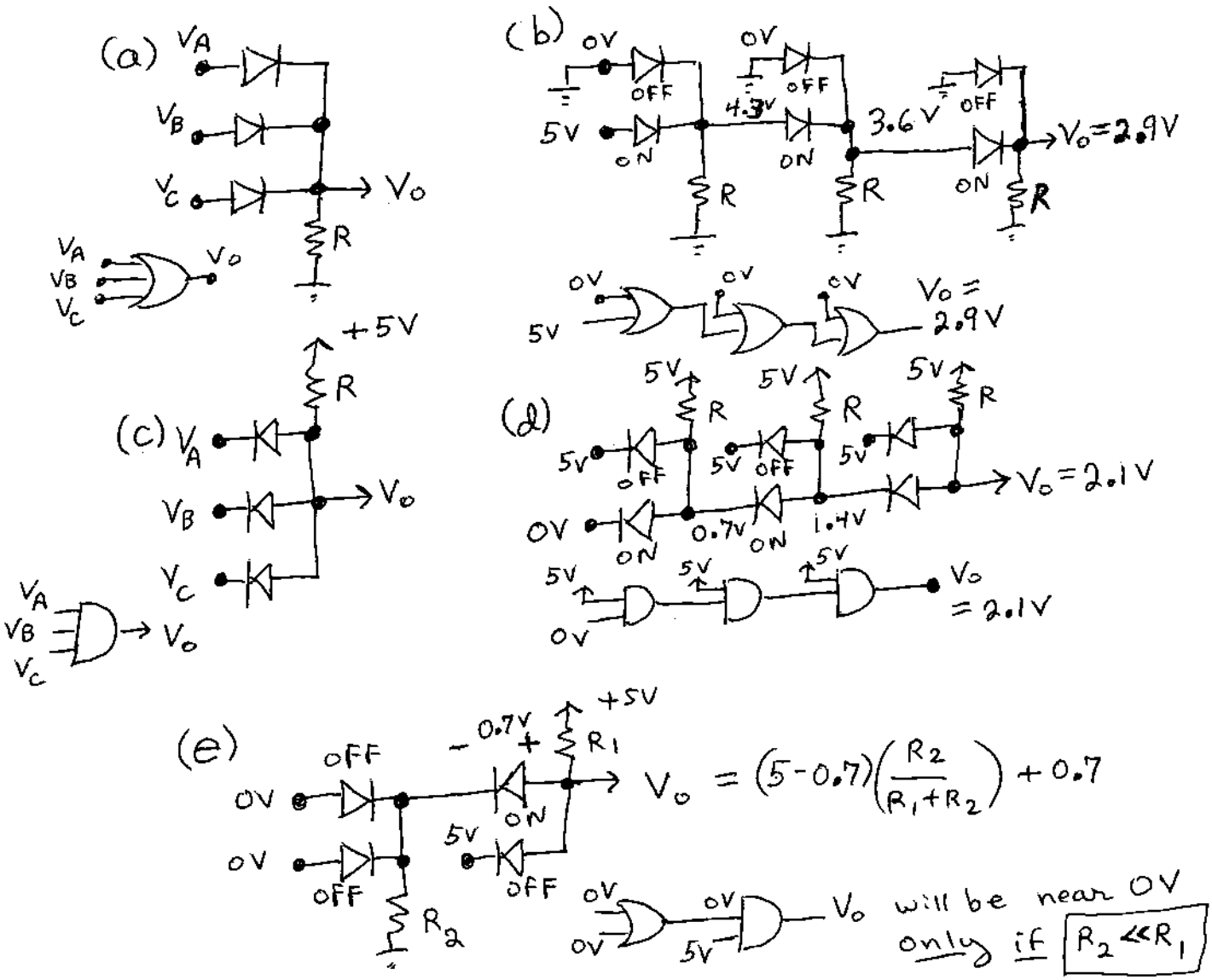


1.11 Diode Logic Circuits

The circuit of a 3-input diode ***OR gate*** is shown in Fig. 1-29(a). Recall that an OR gate develops a low output voltage if all of its inputs are low, but a high output results if any one or more of the inputs are high. In this circuit, if all three inputs are pulled low to 0 V potential with respect to ground, thus all three inputs are said to be "grounded", then all three input diodes will be OFF, and the output will be pulled low (toward 0 volts) through the "***pull-down***" resistor, which is a resistor that has one end tied to the ground (0 V) dc power supply bus. However, if one (or more) of the inputs are high (5 V), then the corresponding diode (or diodes) will be ON, and the output voltage Vo will be at a potential of 5 - 0.7 = 4.3 V with respect to ground, which is still considered to be a valid logic high level.

Note that if a logic HIGH signal is routed through several cascaded OR gates (Fig. 1-29(b)), it will gradually lose its high voltage level, since 0.7 V is dropped for every gate that the high signal travels through. This successive loss of signal level is a significant drawback of (passive) diode logic gates. We will find that combining the diode gates with active amplifying devices (transistors) will solve this signal degradation problem.

Fig. 1-29. Diode Gates. (a) Diode OR gate. (b) Logic High voltage level loss in cascaded OR gates. (c) Diode AND gate. (d) Logic Low voltage level loss in cascaded AND gates. (e) Logic voltage level loss in cascaded diode AND and OR gates.



A 3-input diode AND gate is shown in Fig. 1-29(c). Recall that in a AND gate, all three inputs must be at logic high potential in order to cause a logic high potential to develop at the output. If all three inputs are high (at +5 V), then all three diodes must be OFF, and the output is pulled high (toward +5 V) through the "***pull-up***" resistor, which is a resistor that has one end tied to the +5 V dc power supply bus. If any one or more of the inputs are at logic low potential (say, 0V), then diode corresponding to that input will come ON, and the output will be clipped to 0.7 V, which is still considered to be a valid logic LOW potential.

Note that if a logic low signal is propagated through several cascaded AND gates (Fig 1-29(d)), the logic low signal will gain 0.7 V for every gate it propagates through, thus the logic low level is gradually lost.

Care must also be exercised when cascading a diode OR gate into a diode AND gate (Fig. 1-29(e)). The OR gate pull-down resistor must be made considerably less than that of the AND gate pull-up resistor, so that a sufficiently low logic 0 voltage level can be established at the output of the AND gate. A similar problem exists when cascading a diode AND gate into an OR gate. Now the AND gate's pull-up resistor must be made small compared to the OR gate's pull-down resistor in order to keep the logic high level at a high enough voltage.

The above problems limit the usefulness of diode logic gates to just one one or two levels of cascaded logic without buffering with some kind of amplifying device. Nonetheless, due to their simplicity, diodes have been used along with transistor inverters (to be discussed next week) in implementing ***programmable read-only memories*** (***PROMs***) and ***programmed logic arrays*** (***PLAs***).

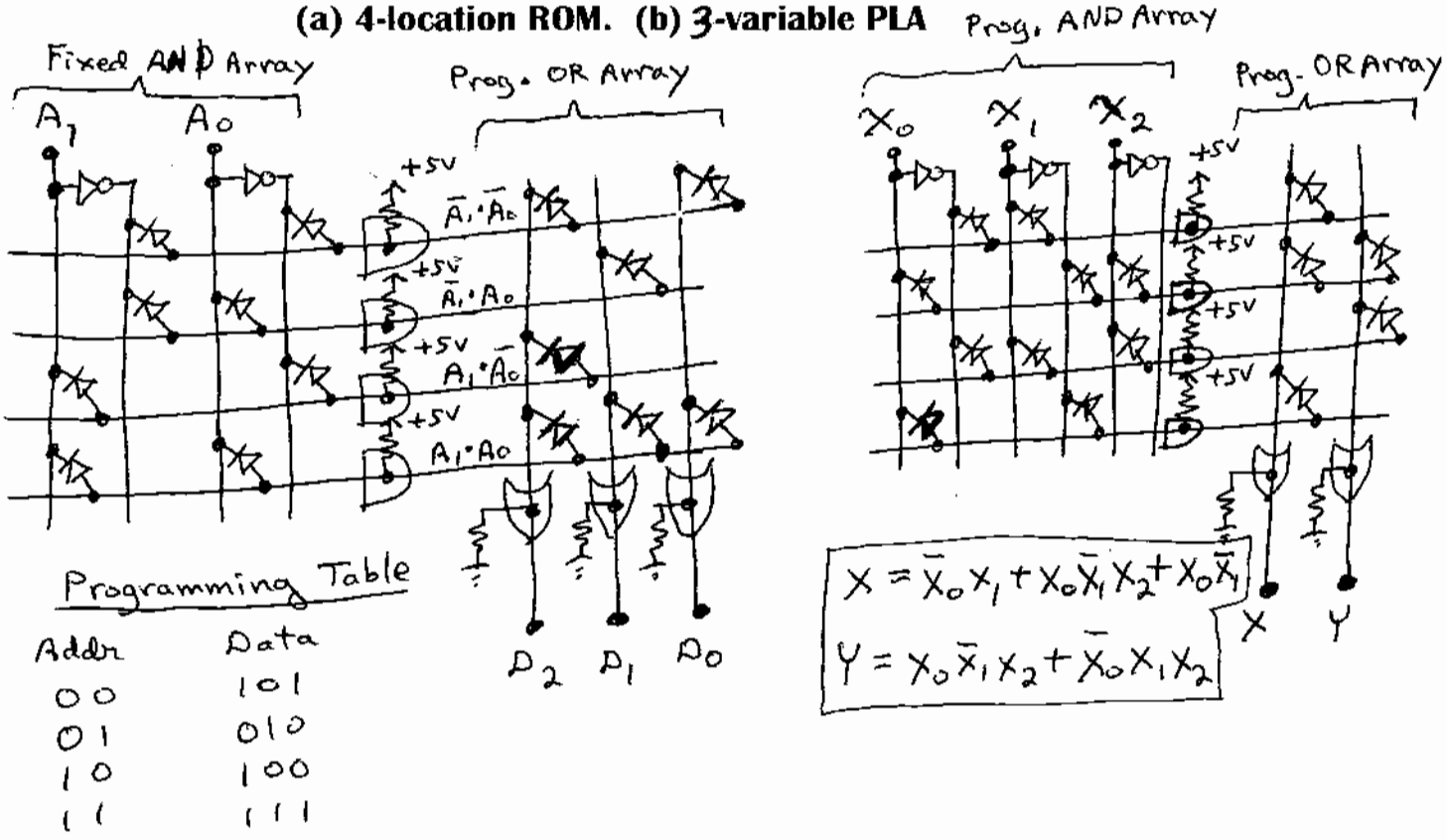
A 4-location PROM and a 3-variable PLA made from inverters, diodes, and resistors are shown, along with their equivalent logic circuits, in Fig. 1-30. Note that both of these circuits consist of a diode AND array (on the left) and a diode OR array (on the right). In the diode AND array, the inputs are brought down as vertical wires in both their asserted and inverted forms. Each of the horizontal lines in the AND array is pulled up to +5 V through a pull-up resistor, and each of these lines corresponds to the output of an AND gate. Any place a diode is present bridging (cathode-to-anode) a vertical input line to a horizontal output line corresponds to an input to the AND gate corresponding to that horizontal line. Thus a product term, made up of one or more asserted or inverted input signals, is formed on each of the horizontal lines.

In the diode OR array, each of the vertical lines (pulled to ground through pull-down resistors) represents the output of a distributed diode OR gate. Selected horizontal product term lines are connected to the inputs of a certain OR gate by the presence of a bridging diod (anode-to-cathode) between the horizontal input line and the vertical output line.

The only difference between the N-input PROM and PLA is that in the PROM, the AND array is fixed, having 2^N horizontal product terms, each one decoding one of the possible 2^N address (vertical input line) values, and the OR array is made ***programmable.*** (Diodes are placed in all possible bridging positions, in series with easily melted wires, called ***fusible links***, so the undesired diodes can be effectively removed from the array at programming time by "blowing out" their fusible links). Each horizontal row corresponds to a different location in the EPROM, and where diodes remain corresponds to a logic 1 in that particular bit position. Each vertical line corresponds to a different EPROM output data line.

In the PLA, on the other hand, there are usually far fewer than 2^N horizontal product term lines, and both the AND and OR arrays are programmable. Thus multiple minimized sum-of-products expressions can be implemented in one PLA. One product term can easily be shared between several outputs, so the use of a ***multiple-output minimization algorithm*** which minimizes all Boolean functions at once, finding the smallest set of product terms (many of which are ***shared*** between various output functions) that ***simultaneously cover*** all of the the specified output functions, rather than independently minimizing each output function in isolation, ending up with perhaps simpler sum-of-products expressions for any one output, but MORE PRODUCT TERMS (horizontal lines in the PLA) will be needed, since it will be unlikely that any of the product terms can be shared. One such multiple-output minimization algorithm is implemented in a program called ***McBoole***, which has been placed in the public domain, and may be copied for private use from our digital lab PCs.

Fig. 1-30. ROM and PLA diode arrays.
(a) 4-location ROM. (b) 3-variable PLA



Programming Table

Addr	Data
00	101
01	010
10	100
11	111

1.12 LED/Photodiode Optical Communication Link

A simple digital optical communication link is shown in Fig. 1-31. The value of current limiting resistor R1 has been chosen to allow the LED's rated forward operating current to flow. If the LED is rated to have full intensity at 50 mA and a forward junction drop of 1.5 V,

$$R1 = \frac{5 - 1.5}{50 \cdot 10^{-3}} \qquad R1 = 70 \quad \text{ohms}$$

The photodiode is reverse-biased so that virtually no current (recall that the reverse saturation current (or dark current) for a typical diode is Is = 1 nA) flows through resistor R2 when no light hits its junction, therefore Vout = 5 V. But when light from the LED hits the photodiode's depletion region, the photons knock loose electron-hole pairs in and near the depletion region, and the reverse-biased photodiode current increases perhaps one-thousand-fold (depending upon the received light intensity). Thus the reverse-biased diode current might increase to 1 μA. If this is true, then Vout will decrease only slightly below the positive power supply level:

$$Vout = 5.0 - 1 \cdot 10^{-6} \cdot 100 \cdot 10^{3}$$

$$Vout = 4.9 \quad V$$

This digital signal is typically coupled through a capacitor (to block the dc offset, which is approximately 5 V), and then amplified to a usable level using a transistor or OP AMP amplifier circuit.

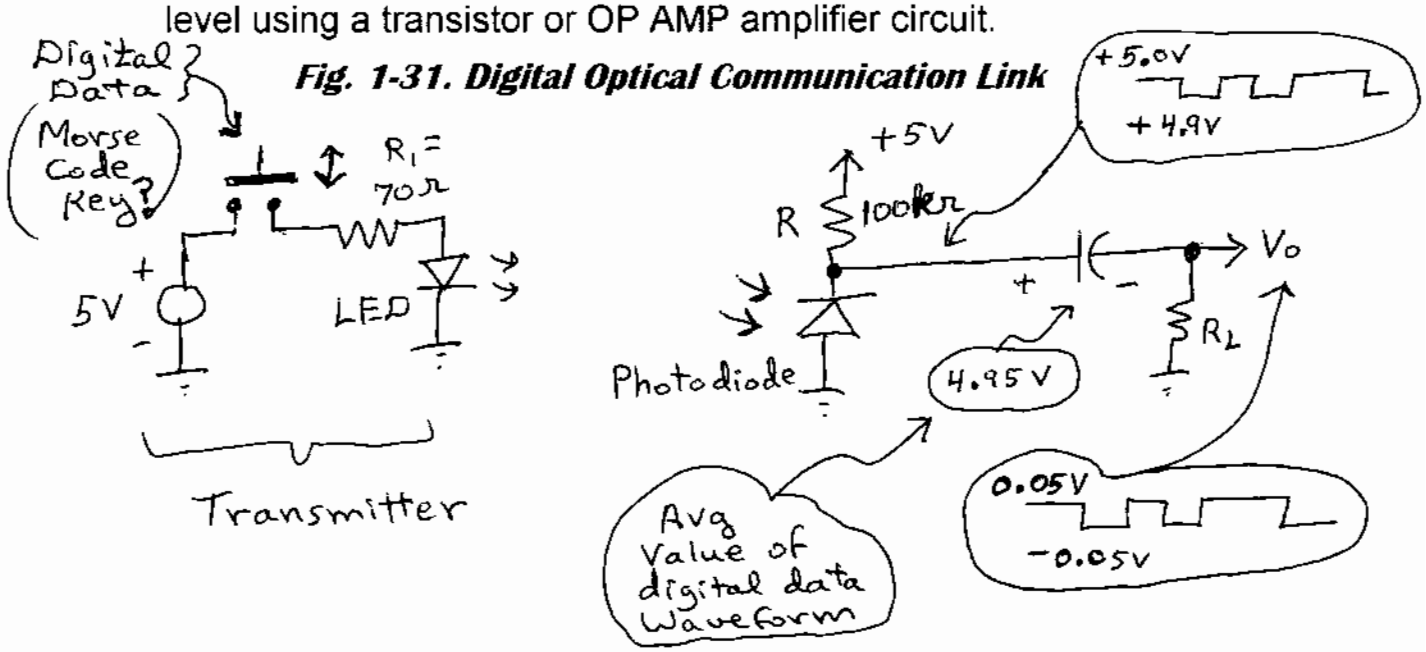
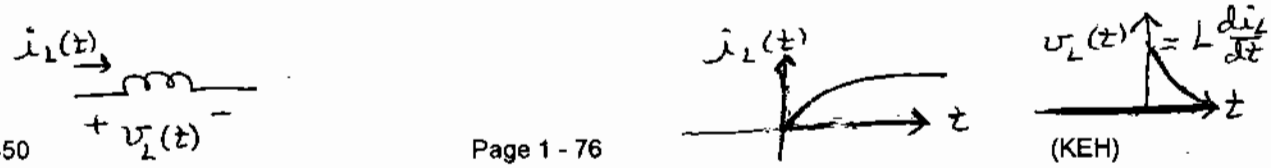


Fig. 1-31. Digital Optical Communication Link



1.13 Diode Suppression of Inductive Switching Transients

Consider the inductive load switching circuit shown in Fig. 1-32(a). The inductive load might be a motor, solenoid, or relay, which is modeled as an inductance, L, in series with a resistance, R. When the switch is ***closed***, current gradually builds up according to the well-known general first-order differential equation RL circuit solution, which holds for t > to:

$$i_L(t) = I_F - \left(I_F - I_I\right)\cdot\exp\left[\frac{-\left(t - t_o\right)}{\tau_{RL}}\right] \qquad \text{for } t > t_o \qquad (1 - 44)$$

where I_F is the final inductor current, (Vs/R)
I_I is the initial inductor current, (0)
t_o is the time that the switch is closed, (0)
τ_{RL} is the RL circuit "time constant", (L/R)

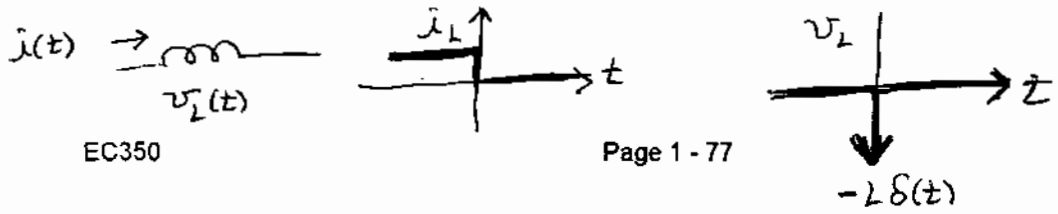
Hence, for our case, (1-45) becomes

$$I_L(t) = \frac{Vs}{R}\cdot\left[1 - \exp\left[\frac{-t}{\left(\frac{L}{R}\right)}\right]\right] \qquad \text{for } t > 0 \qquad (1 - 45)$$

Because the inductor current changes *gradually* (exponentially) between its initial value (0) and its final value (***Vs/R***), there will be no large voltage developed across the inductor during turn-on. The inductor voltage will start at the source voltage level, ***Vs***, then exponentially decay toward zero. This is because the voltage across an inductor is given by

$$v_L(t) = L\cdot\frac{d}{dt}i_L = Vs\cdot\exp\left[\frac{-t}{\left(\frac{L}{R}\right)}\right] \qquad \text{for } t > 0 \qquad (1 - 46)$$

However, when the switch is ***opened,*** say at time ***t = 0***, current immediately falls from **Vs/R** to ***0***, since the switch suddenly breaks the current path.



Thus the current through the inductor is forced to immediately decrease to zero, and di_L/dt is a negative impulse function, then by the first half of (1-46),

$$v_L(t) = -L \cdot \delta(t) \qquad (1 - 47)$$

In reality, the negative voltage spike (called the ***inductive kick***) does not become infinite as (1-47 predicts, since the very high voltage that begins to develop (several hundred volts) across the switch contacts ($v_L(t)$ - Vs) causes a spark to jump between the opening switch contacts (this is called ***switch contact arcing***) that allows the current to decrease at a more gradual rate. Even so, the arcing eventually pits and corrodes the switch contacts, eventually causing the switch to fail.

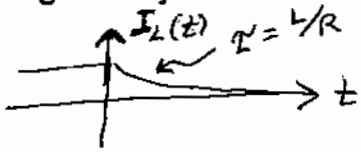
The inductive kick problem can be eliminated by placing a diode across the inductive load, as shown in Fig. 1-32(b). The diode is OFF when the switch is closed, since the voltage across the load is positive. But during turn-off, as the voltage goes negative, the diode comes on and clips the voltage at the safe level of -0.7 V! No contact arcing will result, but it will take some time after the switch is opened for the load current to actually turn off.

The situation is analogous to that of a human (switch) trying to stop a train (the current through an inductor) by brute force (stepping in front of it and pushing). (The inductance of the inductor is analogous to the mass of the train). It is likely that the human will fail to stop the train (and die!), just as the switch will fail due to contact arcing!

But with the diode in place, the human has gotten smart. To stop the train, he switches the train to a circular "run-around" track, and the train will gradually stop.

The inductive load is effectively shorted-out by the diode, and the decrease in load current (after the switch is opened) is given by the general RL circuit formula (1-44):

$$I_L(t) = I_f - (I_f - I_I)\, e^{-(t-t_0)/\tau}$$



$$I_L(t) = \frac{Vs}{R} \cdot \exp\left[-\frac{t}{\left(\frac{L}{R}\right)} \right] \qquad (1-48)$$

Now $I_f = 0$

$I_I = V_S/R$

$\tau = L/R$

It is clear from (1-48) that the rate at which the inductor current decays (the rate at which the "train speed" decays on the run-around track) is set by the time constant L/R, in one time constant, the current has decayed to exp(-1) = 37% of its initial value, Vs/R.

Turn off time can be decreased (at the expense of allowing higher voltages across the switch as its contacts break) by adding an external "turn-off speedup" resistor in series with the diode, as shown in Fig. 1-32(c), thus decreasing the time constant. Now the time constant is decreased to the value $\tau = L / (R + R_{speedup})$.

Fig. 1-32 Switching Inductive Loads (a) without diode transient suppression (b) with diode transient suppression (c) with "turn-off speedup" resistor, $R_{speedup}$.