ECE250 Electronic Device Modeling - Lab #8 NMOSFET Audio Amplifier

(10th Week Demo: Individual Work --- One report per individual!)

ECE Department, RHIT (KEH)

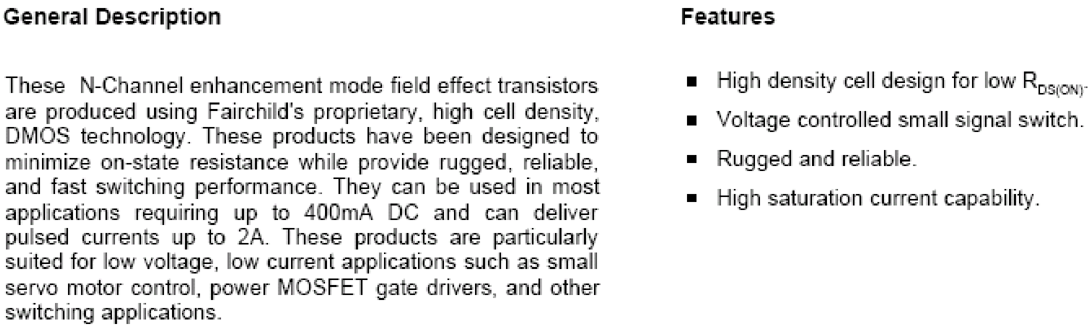
Name: ___________________________ Date: ________

Prelab Assignment: *Assuming that Vtn = 2.2 V and Kn = 46.9* mA/V^2, complete *the PSPICE simulation (See Part 3), and prepare Attachment C* ***before*** *coming to lab. This is mandatory, because your Lab 10 report will be due right after the demonstration is completed.*

The rest of the calculations (Attachments A and B) will be done together during the lab demo. Each student must bring their laptop in order to complete Attachments A and B, and also to complete the ECE250 Opinion Poll during this lab. Also at the beginning of this lab, the Concept Inventory will be re-administered. You will have 50 minutes to complete it, so it is important that you BE ON TIME to lab! It will count 35 points of the 200 point Final Exam (Thus the final exam will be worth 200 – 35 = 165 points.). The concept inventory test will be "curved" in the sense that an additive offset will be added to each of the student's concept inventory exams, so that the highest scoring student will receive the maximum possible score of 35 points.

1) NMOSFET Parameterization – Determining K_N and V_{TN} Using the Curve Tracer

a) The 2N7000 MOSFET was designed for low-power switching applications. It has a transient suppression diode internally connected between its source (S) and drain (D) terminals to provide built-in inductive transient suppression. The 2N7000 is housed in a standard TO-92 plastic package, with a maximum power dissipation rating of 0.40 W, a maximum continuous drain current of Id = 400 mA, a maximum Vds of 60 V, and (Rds)on = 4 ohms. The threshold voltage, V_{TN}, for this part is specified to lie somewhere between 0.8 V and 3.0 V.

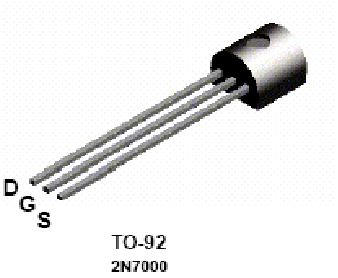


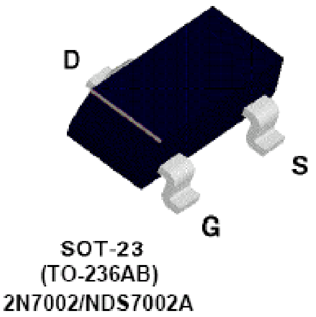
General Description

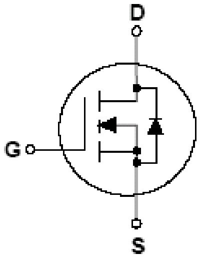
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400mA DC and can deliver pulsed currents up to 2A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.







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Part 1. Measuring V_{TN} and K_N using Curve Tracer

In this first part, you will use the curve tracer to display the Id vs. Vds characteristic curves, and to obtain the conduction parameter, K_N and also the threshold voltage, V_{TN}, for your 2N7000 NMOSFET. The method is outlined in the steps listed below:

Steps for Using the Curve Tracer to Measure $\underline{V_{TN}}$ and **K_N** *of an NMOSFET*

1. Turn on power to curve tracer.
2. Insert the NMOSFET into the socket, where D goes into the C hole, G goes into the B hole, and S goes into the E hole.
3. Select socket (Press the “Left” or “Right” selector buttons at the lower left)
4. Adjust Vertical (Current/Div) knob for 20 mA/div.
5. Adjust Horizontal (Volts/Div) knob for 1 V/Div
6. Adjust Step/Offset Amplitude knob by turning it to the left (CCW) to select voltage steps, as opposed to selecting current steps by turning it to the right (CW), as we did before when we were curve tracing BJTs. Select 500 mV/Step.
7. Select the number of steps to be “10”, using the paddle located to the left of the Step/Offset Amplitude knob.
8. Increase the collector supply “MAX PEAK POWER WATTS” paddle to “2” amperes.
9. Advance “Collector Supply Variable” knob located at the lower right of the pane until one or more non-zero Id vs. Vds curve(s) can be seen above the Vds (Id = 0) axis.
10. Decrement the Number of Steps using the paddle located to the left of the Step/Offset Amplitude knob until *only one* curve above the Vds axis is visible. This is the first curve whose Vgs value has gotten above the NMOSFET threshold value, V_{TN}. Determine the value of Vgs that corresponds to this curve by reading the Step Number using the scale to the left of the selection paddle. Let us imagine the number of steps is “5”. Then you may determine Vgs by multiplying by the Voltage/Step setting (in this case = 500 mV). Thus in this example,
    $$Vgs = 5*500mV = 2.5\ V$$
11. Now press the “Oppose” button that is located directly below the Step/Offset Amplitude knob. This button decrements the Vgs voltage step values by the constant offset indicated as “offset” on the scope display. Repeatedly press this button until the curve falls to the Id = 0, or Vds, axis. Read the “Offset” voltage from the display. Let us imagine it is -300 mV. Then we may calculate the NMOSFET’s threshold voltage as
    $$V_{TN} = 2.5\ V – 300\ mV = 2.2\ V$$
12. Depress both the “Oppose” and the “Aid” buttons simultaneously to cancel this offset and to allow the curve to return to its normal position. You may press the Number of Steps of paddle to add more steps to the family of curves. You may have to adjust the sensitivity of your Id axis as needed, and you may want to increase the maximum power setting (using the paddle at the bottom right), in order to display several curves from this family
13. Now that the threshold voltage,V_{TN} has been determined, we next measure the conduction parameter, K_N. Do this by measuring a point (Idx, Vdsx) on the flat part (saturation region) of an Id vs.Vds curve corresponding to Vgs > V_{TN}. In this example, let us follow the Id vs. Vds curve corresponding to Vgs = 3.0 V out to Vds = 4 V, which is guaranteed to be well into saturation, since Vgs – Vds = 3 – 4 = -1 V < $V_{TN =}$ 2.2 V. Imagine that we measure Id = 32 mA at this point. Thus we can calculate KN using the saturation mode formula for Id:
    $$Id = K_N *(Vgs – V_{TN})\hat{}2 \;\Rightarrow\; 32\ mA = K_N *(3\ V – 2.2\ V) \Rightarrow K_N = 50\ mA/V\hat{}2$$
14. Finally, calculate the value of VM = 1/λ for the NMOSFET. Do this by calculating the slope of the straight part of the Vgs = 3 V curve the slope of this curve. For example, imagine that Id is measured to rises by ΔId = 0.2 mA over a run of ΔVds = 5 V, ΔVds / ΔId = V_M/Idx, and substituting in numerical values we have V_M = (32 mA)*5V/0.2mA = 800 V.

Follow the steps outlined above to use the curve tracer to measure the threshold voltage ***V_{TN},*** *conduction parameter* ***K_N*** *, and the V_M, of your own 2N7000 NMOSFET in the vicinity of the Q-point we will be using, showing your calculations for each of these parameters in the space below.*

Calculation of measured V_{TN}, K_N, and $V_M = 1/\lambda$ from Curve Tracer Measurements

V_{TN} = __________ V
K_N = __________ mA/V^2
V_M = __________Volts

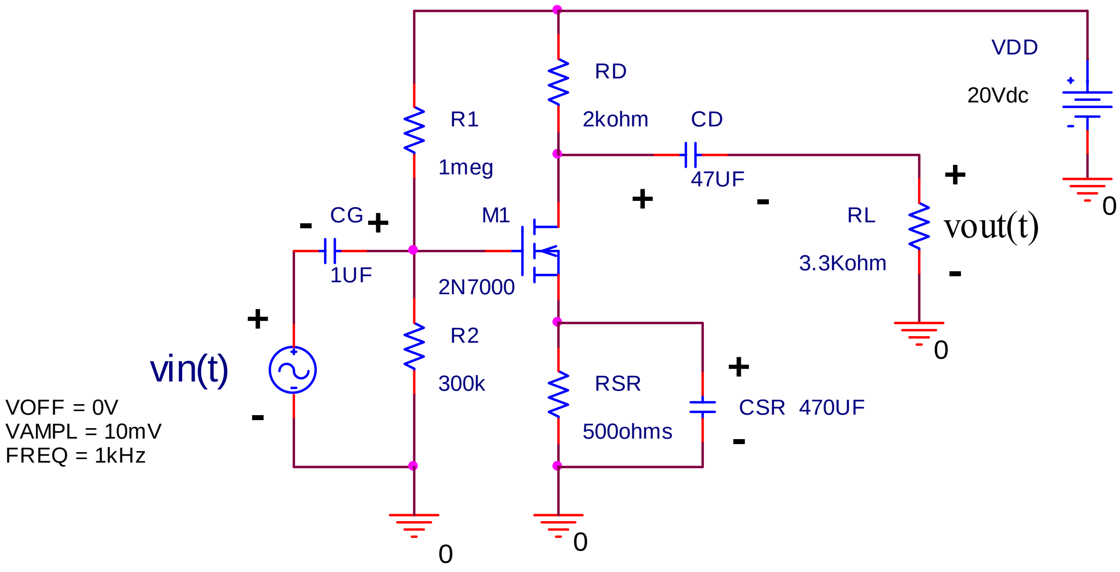
Part 2. Hand Calcuations

(A) ***DC Hand Analysis***: Consider the circuit of Fig.L8-1. Using the MOSFET parameters you measured in Part 1, determine the Q-point (Vgsq, Vdsq and Idq) via hand calculations. Include these calculations as ***Attachment A***. You may assume that the MOSFET is operating in its saturation region. After you determine the Q point, demonstrate that the MOSFET is really operating in its saturation mode by calculating (Vgsq – Vdsq) and compare this value with V_{TN}. Fill in the blanks below:

Predicted Vgsq = __________
Predicted Vdsq = __________
Predicted Idq = __________

(Vgsq – Vdsq) = __________ < V_{TN} = __________ => saturation mode

Figure L8-1 NMOSFET Common-Source Amplifier Circuit



(B) ***AC Hand Analysis***: Calculate gm and also ro based on the Q-point calculated in Part A, and also "hand-calculate" the unloaded voltage gain, Avo, input resistance Rin, and the output resistance, Rout. Then calculate the *loaded* voltage gain, Av. Finally, calculate the maximum output voltage swing (with the 3.3 kilohm load resistor in place.) Include these calculations as ***Attachment B***, and also fill in the results of these calculations in the space below.

gm = _________ mA/V ro = ____________ kΩ

Avo = _________ (with RL removed)

Rin = _________ kilohms

Rout = _________ ohms

Av = _________ (with RL in place)

Max Symmetrical Output Voltage Swing = _________ V peak-to-peak

Part 3. PSPICE Analysis

Use PSPICE to perform a transient (and a dc bias-point) analysis using the NMOSFET parameters that you measured in Part 1 (assume the values you will measure are given in the prelab assignment at the beginning of this document). Include your PSPICE schematic, with the "V" and "I" buttons pressed in order to show the DC quiescent bias voltage and current values on the schematic. Also include your transient analysis plot, with voltage probes placed at the input and output. These two PSPICE results should be placed in your lab report as ***Attachment C***. *Remember to use the IRF150 NMOSFET model, with the PSPICE parameter VT0 set equal to your measured* V_{TN} *threshold value, and with the PSPICE "process gain" parameter KP set equal to your measured* K_N*, and with W = 2U (2 microns) and L = 1U (1 micron), as discussed in class.* By pressing the "V" and "I" PSPICE buttons, you can measure the simulated DC (quiescent bias point) values in the circuit, and you can perform a transient analysis similar to the NMOSFET simulation example that was distributed in class in order to determine the loaded gain. From this simulation, fill in your simulation results in the middle column of Table 1 below, and compare with the hand-calculated results from Part 2 and the measured results from Part 4. Your PSPICE simulation should start with a relatively low-amplitude (1 mV) input sine wave, at a frequency of 1000 Hz. Once the loaded gain is found, you must gradually increase this amplitude in order to determine the maximum symmetrical output voltage swing using PSPICE. *Hint: your PSPICE analysis should reveal Vgsq = 2.50 V, Vdsq = 9.42 V, Idsq = 4.23 V, Av = -34.7, and a maximum symmetrical Vds swing of approximately 13.8 V. Everyone should get these same results, except for the maximum symmetrical swing, which is a bit of a judgement call.*

Part 4. Observed Results

Now build the circuit, measure the DC Q point values and use a function generator whose output has been set to deliver a 1000 Hz sine wave with a relatively low voltage amplitude (say 100 mV) that will allow you to experimentally measure the loaded voltage gain Av. Then gradually increase this input amplitude as you experimentally measure the maximum symmetrical output voltage swing.

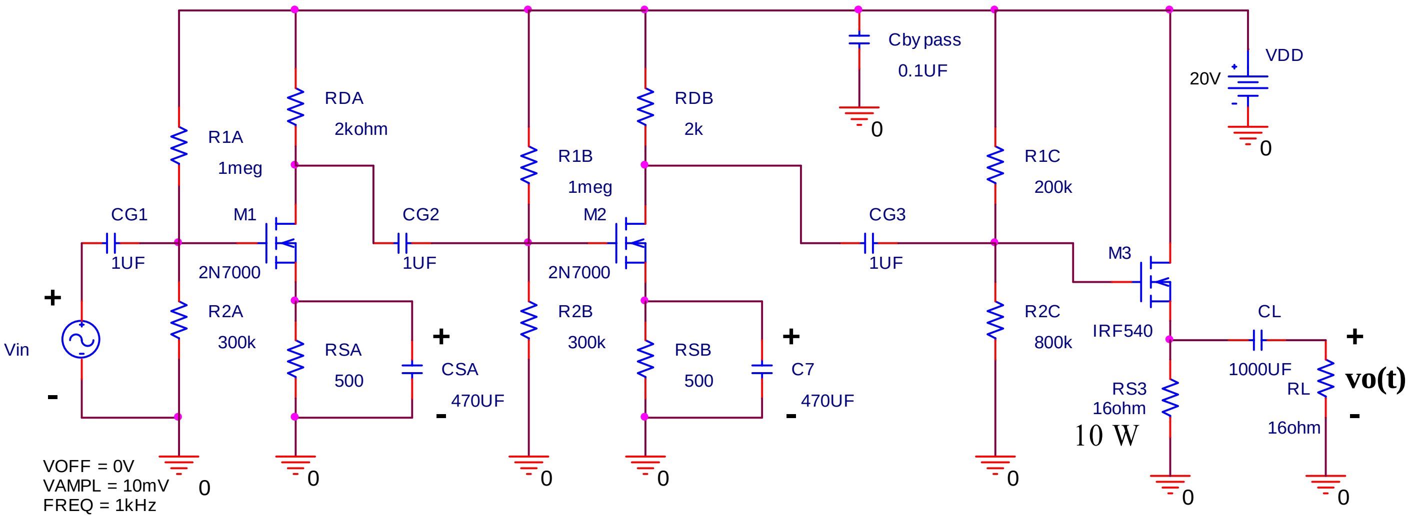
Table 1. Summary of results from hand calculations, PSPICE simulations, and experimental observations

	HAND CALCULATED	PSPICE SIMULATION	OBSERVED
Vgsq			
Vdsq			
Idsq			
Av			
Max Sym Swing			

Part 5. MOSFET Audio PA System

Figure L8-2 below depicts a complete audio public address (PA) amplifier system consisting of two common-source voltage amplifier stages identical to the one analyzed above, and one common-drain (source follower) current amplifier stage with high input impedance and low output impedance suitable for allowing a microphone input and an 8-ohm or 16-ohm loudspeaker load.

Figure L8-2. Complete MOSFET Audio PA System consisting of two common-source voltage amplifier stages identical to the one analyzed above, and one common-drain (source follower) stage with high input impedance and low output impedance suitable for driving the 16-ohm loudspeaker load.



Since each of the two common-source voltage amplifier stages has a voltage gain of about -32, then the overall voltage gain provided by the two voltage amplifier stages is (-32)*(-32) = 1000. The common-drain (source-follower) output stage has an open circuit voltage gain of unity, and a relatively low output impedance of around 16 ohms. Thus the overall voltage gain with RL = 16 ohms is approximately Avtot = vo/vin = 32*32*1*(16/(16+16)) = 512.

Note that the power supply must be capable of supplying up to one ampere, RS3 must be a 10 Watt resistor, and M3 must be attached to a “heat sink”, as its dc bias Q-point is approximately Vds3q = 11 V and Id3q = 0.55 A. Thus the electrical power dissipated in M3 (even with NO ac signal being amplified) due to biasing M3 at this Q point is P3q = Vds3q*Id3q = 6.05 W. The maximum undistorted symmetrical swing is approximately 12 V peak-to-peak, so the output audio signal power delivered to the 16 ohm load (loudspeaker) is

PL = vo(rms)^2 / RL = ((12/2)*0.707)^2 / 16 = 1.2 Watts

Clearly this is not a very efficient audio power amplifier, since the dc bias (Q) point power consumed is 6 Watts, and the output audio signal power is only 1.2 Watts.

We could do much better by going to a complementary symmetry common drain (source follower) output stage consisting of an NMOSFET and a PMOSFET arranged in a configuration similar to that of Lab 7.

In lab we shall re-measure these power consumptions and re-calculate the dc supply power and and also the ac signal power discussed above.

Observed DC Power = Vdd * Idd = ______W   IRF540 DC Power = Vds3q*Id3q = ______ W

Observed max undistorted symmetrical output voltage swing = __________ V, pp

Observed maximum undistorted output (AC) signal power delivered to 16-ohm load = _________ W

Power Efficiency = Ratio of AC Signal Power to DC Supply Power = ________