ECE250 Lab Project #6
Design of a Common-Emitter Audio Amplifier

April 23, 2010 (KEH)
Department of Electrical and Computer Engineering
Rose-Hulman Institute of Technology

Lab Team Members: _____ _____
Date Performed: _____ Lab Station: _____

In this experiment you will first measure the beta of your transistor, design the amplifier circuit below (by calculating the necessary values of R1, R2, RC and RE) to exhibit a specified dc Q-point, investigate Q-point stability with respect to β using circuit analysis, and finally predict the small-signal voltage gain and maximum symmetrical output voltage swing, and then compare your predictions against measured and simulated values.

PRELAB ASSIGNMENT:

Since you won't know the precise value of β for your specific transistor ahead of time, assume β = 200 when working through this prelab. In this prelab, please create a Maple worksheet with β as a variable that is defined at the top of the worksheet, so that you can simply change the value of β in the worksheet to recompute all the necessary values once you have measured the precise value of your BJT.

1) Consider the common-emitter (CE) amplifier circuit shown in Fig. L6-1. Assume that V_{BEON} = 0.7 V, and that the (dual) dc power supplies are Vcc = +12 V and Vee = -12 V. The desired dc bias Q-point is ***I_{CQ} = 15 mA and V_{CEQ} = 11 V***. Note that when you Theveninize the base bias circuit, you may use Linear Superposition to find Vth = $V_{OPEN\ CIRCUIT}$. You should be able to show, using Linear Superposition, that

$$Vth = (+12)\frac{R2}{R1+R2} + (-12)\frac{R1}{R1+R2}$$

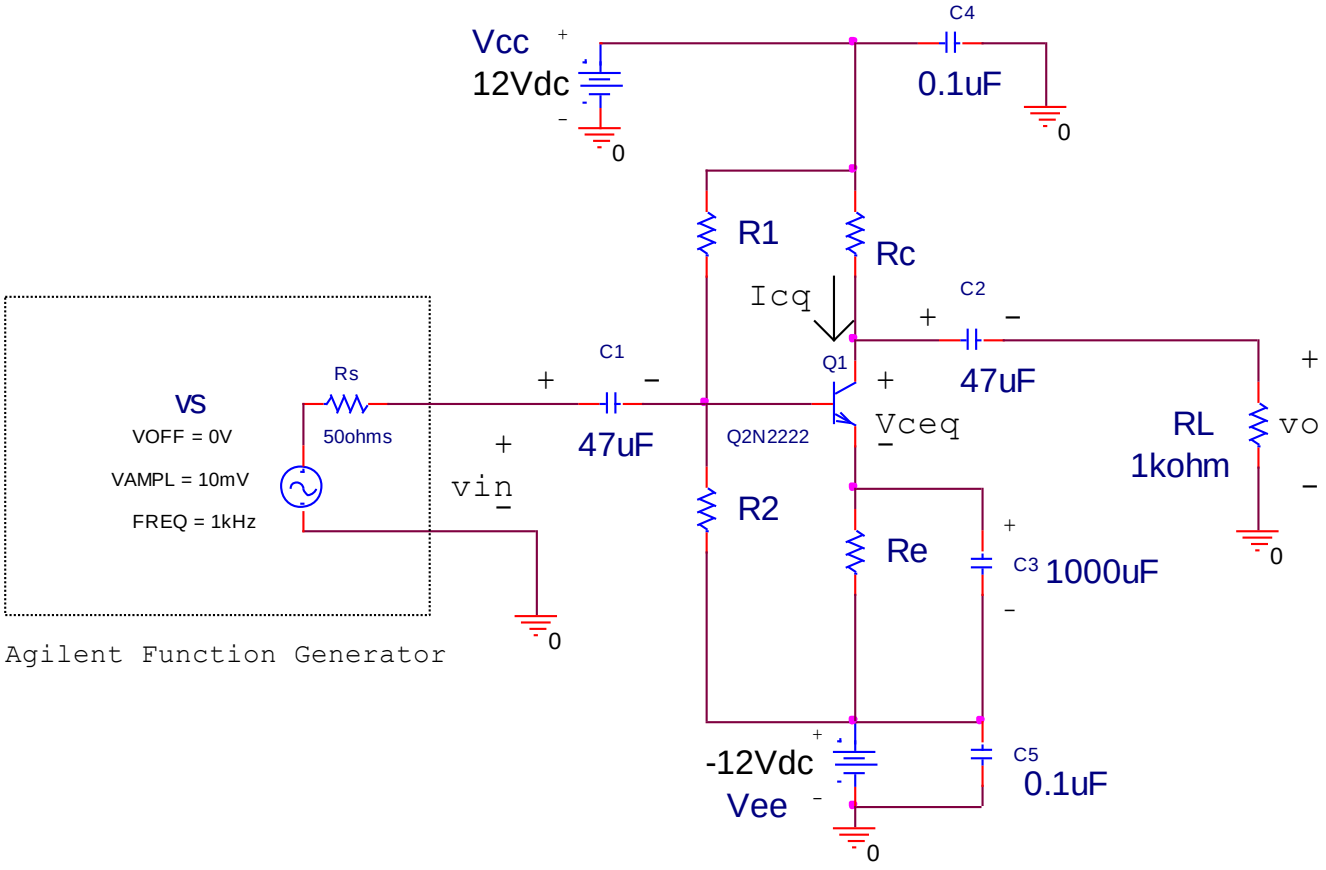
Note that the negative side of Vth connects to GROUND, not either Vcc = +12 V or Vee = -12 V. Note that Rth is still R1 // R2, after you set the two dc power supply sources to zero.

Alternatively, we may find Vth = $V_{OPEN\ CIRCUIT}$ without using Linear Superposition by writing the following node equation at the junction of the R1 and R2, assuming that the base of the BJT has been temporarily disconnected:

$$(Vth - 12)/R1 + (Vth - (-12))/R2 = 0$$

Solving this equation for Vth should yield the same result as obtained using Linear Superposition.

Fig. L6-1. Common Emitter (CE) NPN BJT Audio Amplifier



a. Design the circuit so that V_{RC} = 12 V, Vce = 11 V, and V_{RE} = 1 V using the rule of thumb that Rth = $0.1(\beta_F+1)$Re for good bias stability. Attach your calculations as **Exhibit A1**. (Remember units!)

Results: R_E = _____ R_C = _____ R_1 = _____ R_2 = _____

b. Now investigate the stability of this Q-point with respect to variation in β_F by recalculating the Q-point for β_F = 100 and for β_F = 300, keeping the four resistors the same as in Part (a). Attach your calculations as **Exhibit A2**. (Remember units!)

Results: For β_F = 100 I_{CQ} = _____ V_{CEQ} = _____
For β_F = 300 I_{CQ} = _____ V_{CEQ} = _____

c. Calculate below the small-signal transistor parameters: r_π & g_m that corresponds to the Q point when β=200. Assume the 2N2222 BJT exhibits ***n = 1.3*** (since this is a discrete BJT, as opposed to an IC BJT as in our textbook where n = 1.0), and room temperature conditions, ***V_T = 26 mV*** (Remember units!).

Result: r_π = _____ g_m = _____

d. Draw an AC circuit model of the BJT amplifier in the space below with emitter bypass capacitor C_E in place and then a second AC model with C_E removed.

AC Model of CE Amplifier Circuit of Fig. L6-1 with C_E in place

AC Model of CE Amplifier Circuit of Fig. L6-1 with C_E Removed

2) With the emitter bypass capacitor in place, use the first AC model drawn above to calculate the small-signal open-circuit (unloaded) voltage gain, A_{V0}; the small-signal input resistance, Rin and the small-signal output resistance, Rout. Also determine the (loaded) transducer voltage gain Avt = vo(t)/vin(t). Recall that Avt = Avo*RL/(RL+Rout). Attach your work as **Exhibit A3**.

   Predicted Results: A_{V0} = _____ Rin = _____ Rout = _____ Avt = _____

3) Next, remove the emitter bypass capacitor. Using the second AC model drawn above, calculate the small-signal open-circuit (unloaded) voltage gain, A_{V0}; the small-signal input resistance, Rin and the small-signal output resistance, Rout. Also determine the (loaded) transducer voltage gain Avt = vo(t)/vin(t). Recall that Avt = Avo*RL/(RL+Rout). Attach your work as **Exhibit A4**.

   Predicted Results: A_{V0} = _____ Rin = _____ Rout = _____ Avt = _____

Perform two PSPICE transient simulations of your circuit (one with the emitter bypass capacitor C_E present, and one with C_E removed).

Use the "***Q2N2222***" transistor model found in the ORCAD 9.2 Lite Edition PSPICE's "***EVAL***" library. Be sure to modify the β_F parameter that is called "***BF***" in the PSPICE model to match the β_F value that we are assuming in this prelab (BF = 200). Do this by single left clicking directly on the BJT symbol until a pink dotted square selection box surrounds the entire BJT symbol. Then single right click inside this box and select "***Edit PSPICE Model***" from the menu box that appears. After changing this entry, be sure to click on ***File – Save*** in order to save this change you have made to the Q2N2222 device model in the PSPICE EVAL library. Later, after you have

measured your own BJT from the curve tracer, please rerun this simulation with the updated value of BF corresponding to your own transistor.

Include (1) your PSPICE schematic diagram and (2) your PSPICE transient analysis (PROBE) plot of vin(t) and vo(t) with maximum and minimum values of both vin(t) and vo(t) labeled using the "*Mark Cursor*" button icon, as discussed in our first lab. Present your simulated results for the fully bypassed case (C_E present) as **Exhibit B1**, and the unbypassed case (C_E removed) as **Exhibit B2.** Fill in the blanks below with the V_{CEQ} and I_{CQ} values (which can be read by pressing the "V" and "I" button icons) Calculate the percent deviation from the hand calculated (predicted) values for V_{CEQ}, I_{CQ}, and also calculate the simulated Avt = vo(t)/vin(t). Compare these PSPICE simulated results for Avt with the predicted value of Avt obtained in Part 3 above. ***The PSPICE simulated Q point and Avt values should lay within 20% percent of the hand calculated values.***

	C_E Present		**C_E Removed**	
PSPICE RESULTS:	***VCEQ=_____***	***ICQ=_____***	***Avt = _____***	***Avt=_____***
Hand Calculations:	***VCEQ = 11 V***	***ICQ= 15 mA***	***Avt = _____***	***Avt=_____***
Percent Deviation:	_____	_____	_____	_____

END PRELAB

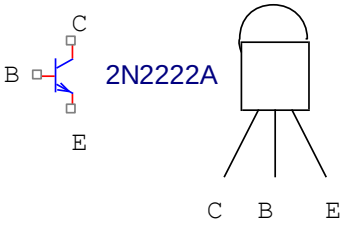
Prelab Answers (Parts 1 – 3)

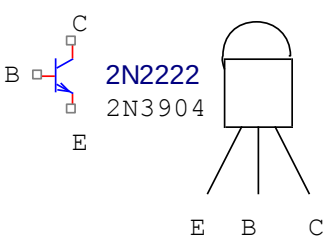
(Exhibit A1) Re = 66.33 ohms, Rc = 800 ohms, R1 = 17.777 kohms, R2 = 1.441 kohms

(Exhibit A2) For beta = 100, Q-point changes to Vceq = 12.128 V and Icq = 13.69 mA
For beta = 300, Q-point changes to Vceq = 10.57 V and Icq = 15.49 mA

(Exhibit A3) with CE (emitter bypass capacitor) in place: Avo = unloaded transducer gain, with RL removed = -355
rout = Rc = 800 ohms
rin = 336.82 ohms
Avt = loaded transducer gain, with RL in place = -197.2

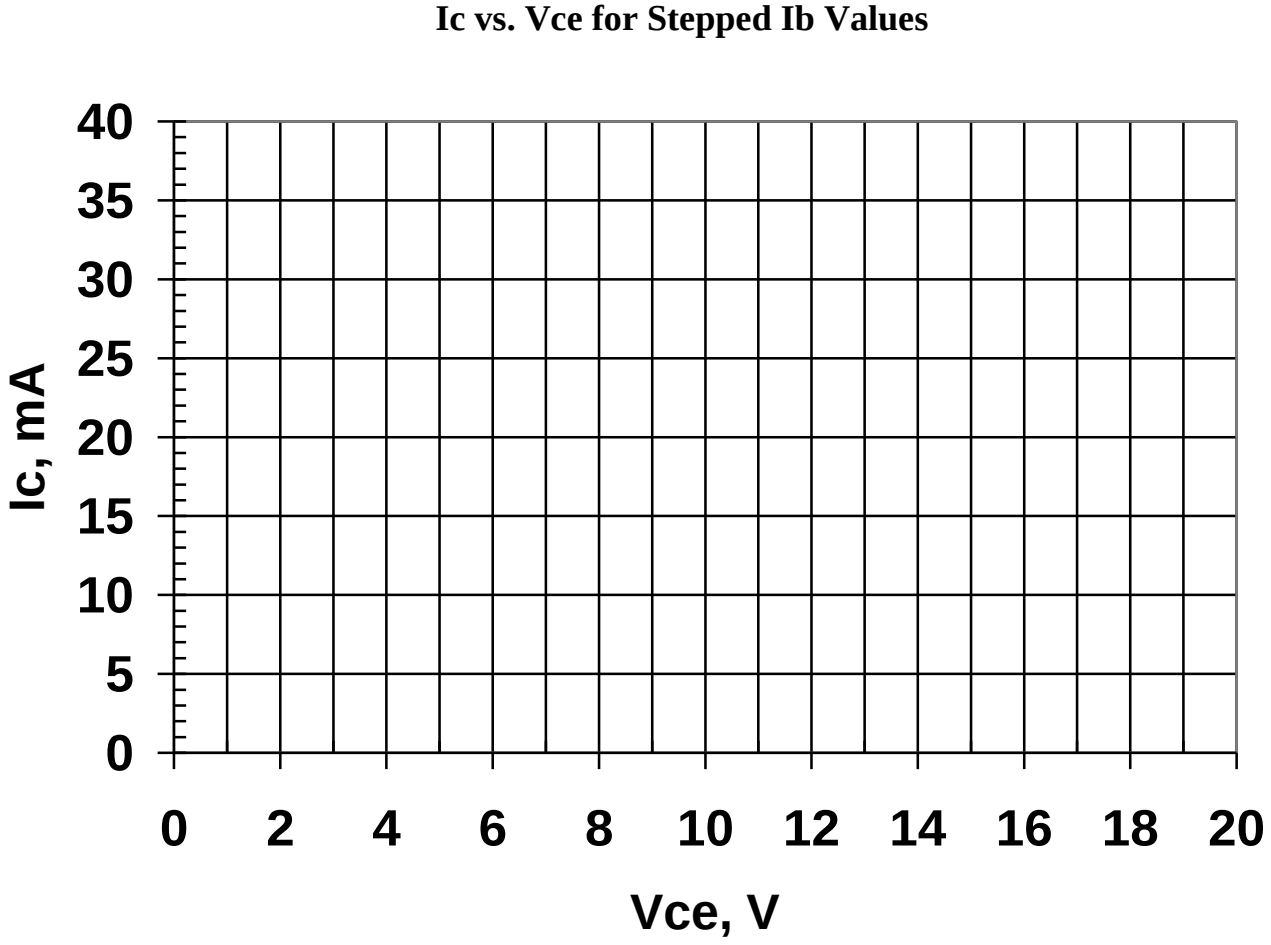
(Exhibit A4) with CE removed:
Avo = -11.61
rin = 1.215 kohms
rout = 800 ohms Avt = -6.4





1) Following the instructions in the attached document in Appendix A, "Using the Sony-Tektronix 370 Curve Tracer to Trace Common-Emitter Ic vs. Vce curves of an NPN BJT", display the collector characteristics (Ic vs Vce for stepped values of Ib) for a 2N2222 BJT using the curve tracer in the laboratory. (The physical pin-out of the 2N2222 is shown above.) Include a suitable sketch of these characteristics in the space below - be sure to mark the corresponding Ib value on each of the curves. From this sketch, determine an approximate value of $\beta_F = \Delta Ic/\Delta Ib$ roughly in the vicinity of $\mathbf{I_{CQ} = 15\ mA}$ and $\mathbf{V_{CEQ} = 11\ V}$. Select a 2N2222 BJT with a β_F that lies above 180, if possible.)

Sketch of BJT CE Collector Characteristics for Your 2N2222 Transistor
(DC and AC Load Lines to be drawn on this plot later in this lab)



Result: Measured value of β_F at Q point (I_{CQ} = *15 mA and* V_{CEQ} = *11 V*) = _____

Adjust the value of β_F in your MAPLE worksheet to match the measured result found above (**Exhibit A**), and attach your modified worksheet as **Exhibit C**.

2) Now use the values calculated in ***Exhibit C*** to carefully and neatly build this circuit on your prototyping breadboard using the nearest available standard resistor values. A photograph of a similar (but not identical) breadboard appears in Fig. L6-2.

   There are several breadboarding rules that I will be requiring you to follow in this course from now on, which are illustrated by Fig. L6-2:

   a. In a circuit with a single dc power supply**,** *always* use the red power distribution bus at the top of your breadboard for the Vcc dc power supply bus; likewise *always* use the blue power distribution bus at the bottom of your breadboard for the ground (0 V) bus. In a circuit with TWO dc power supplies (as in this lab), please use the top red bus for the Vcc = 12 V dc supply, the bottom red bus for ground (0 V), and the bottom blue bus for the Vee = -12 V dc power supply. *Never* use the horizontal distribution busses for any other purpose except for dc power distribution. If you pass an input or an output signal on these busses, you are increasing the chance of capacitive coupling between input and output terminals of your amplifier, and therefore promoting the chances of undesired oscillation.

   b. *Always* place an ac transient bypass capacitor (0.1 μF) across the Vcc dc power bus and ground bus (and in the case of dual-dc supply circuit such as this one, across the Vee and ground bus as well). Note the capacitors C4 and C5 perform this function in Figure L6-1. These capacitors are used to absorb power supply noise caused by sudden switching transients inside the devices that are powered on the breadboard. Recall that capacitors will not pass dc, but will pass ac (noise), so the dc power is not affected by these capacitors, but any ac noise on the dc power bus will be shorted to ground by these capacitors. Sudden Vcc or Vee current demands made by one device on your breadboard can cause momentary voltage drops on your breadboard due to the self-inductance of the power distribution wires if this capacitor is not installed. Such voltage drops can make your circuit randomly malfunction, and sometimes even break into undesired oscillation. Here is a helpful analogy: Have you ever been in the shower when your roommate flushed the toilet? Ouch! The sudden cold water (current) demand made by the toilet as it flushes causes a sudden pressure (voltage) drop in the cold water supply (dc power bus) pipe, which makes a neighboring device, in this case the shower, that is also connected to the water supply pipe malfunction, resulting in your getting scalded! This is due to the inertia of the water (inductance of the dc power bus wires) and the narrowness and length of the water supply pipe (resistance of the dc power bus wires). The solution? Add a "local reservoir of charge", that is, a small water tank (an ac bypass capacitor) *near the toilet* to locally supply the sudden water demand made by the toilet as it flushes. Now the water pressure in the pipe will not momentarily fall as the toilet is flushed, allowing the shower to continue working properly. Of course, it is important that the toilet not be flushed again until the small reservoir (capacitor) has time to recharge at a slow rate that does not cause a large pressure drop on the water pipe.

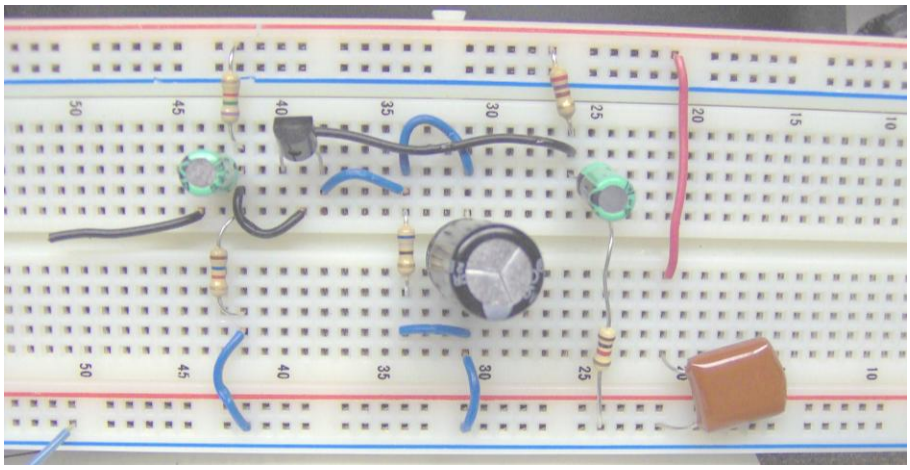
   c. *Always* cut your resistor and capacitor component leads *short* in order to minimize the amount of bare wire that is exposed on the board. Then interconnect your components with reasonably short lengths of insulated hookup wire. Note how this rule has been followed in Fig. L6-2. Please note that this figure is NOT the exact circuit you are wiring, but it is a very similar one!

d. *Never* wire a lot of components directly to the terminals of the transistor, as this will result in a cluttered area that may lead to an undesired short-circuit. Also, keeping your transistor clear of many other components makes it easier to change out the BJT, or to probe the terminals of the BJT during circuit debugging. Instead, run a single wire from each transistor terminal over to a less crowded area of the breadboard, where the components can be located. See, for example, how the base bias resistors (R1 and R2) and the input coupling capacitor (CB) have been moved off to the left of the BJT in Fig. L6-2. Note how the collector pull-up resistor and the output coupling capacitor and the load resistor (RC and CC and RL) have been moved off to the right of the BJT. Similarly, note how the emitter resistor and the emitter bypass capacitor (RE and CE) have been placed well away from the BJT on the breadboard.

e. *Never* try to bend the BJT leads into a different order, but rather keep them in the same order that they come out of the BJT case. If you try bending the leads into a new order, you will likely short out two of the three BJT terminals, which could possibly burn out the BJT!

f. *Always* observe the polarities of electrolytic capacitors (CB, CC, and CE). The (+) terminal must connect to the node that is at the higher average dc potential, in order for the electrolytic capacitor to maintain its dielectric so that it will function properly.

Figure L6-2 Photograph of a SIMILAR (But not identical) CE Amplifier Circuit (Keep your wires short, component leads cut short, etc.)



3) With the function generator ***OFF***, use your bench DVM to measure the dc Q-point. Do this by directly measuring V_{CEQ} and V_{BEQ}. Then indirectly measure I_{CQ} by measuring the voltage across R_C, and then divide this voltage by R_C to obtain I_{CQ}. How close did your measured Q-point come to the desired design goals that you started with in Part 2? ***(NOTE: Because your resistor values will be only + or – 10% of the calculated values, and because you are using the simplest possible BJT model, if you are within plus or minus 20% of the design value, you are fine!)***

Measured Results: V_{BEQ} = _____ V_{CEQ} = _____ I_{CQ} = _____

Design Goals	0.7 V	11.0 V	15 mA
Percent Deviation:	_____	_____	_____

Note: *WHEN TROUBLESHOOTING ANY BJT AMPLIFIER, YOU SHOULD ALWAYS CHECK THE DC OPERATING Q-POINT FIRST BEFORE BOTHERING TO CHECK ITS AC PERFORMANCE, SINCE IF THE Q-POINT IS WAY OFF, THERE IS NO WAY THAT THE AC PERFORMANCE WILL BE CORRECT!*

4) Now you must set up your Agilent function generator to "***Hi-Z***" output mode, as was done in the previous lab project. Now set your function generator so that it delivers a ***10 mV peak-to-peak***, ***1 kHz*** sine wave when the function generator is connected across the input terminals of the amplifier. Next, connect the function generator to the input terminals of your amplifier circuit (making sure that dc power has been applied to your circuit), and place an oscilloscope probe across the generator terminals in order to monitor the input voltage, vi(t), delivered to the input terminals of the amplifier. You will find that "***autoscale***" does not work with such low signal levels, so you will have to manually adjust the channel sensitivity and sweep rate knobs in order to display the signal. You will probably find that the 10 mV peak-peak sine wave input signal displayed on the oscilloscope is quite "fuzzy". This is because there is a large amount of high-frequency radio interference present on the Rose-Hulman campus, probably due to nearby computers. In order to remove this high frequency noise, we may average several (say 64) samples of the vi(t) waveform. This averaging process will preserve the periodic signal, which adds *coherently* from one sample to the next, assuming that the signal has been properly triggered, so that the displayed periodic waveform is stationary. The high frequency noise, on the other hand, will add *incoherently*, and thus will be largely cancelled out in the averaging process.

   To use the signal averaging feature of the Agilent 54622D digital oscilloscope, first make sure that the unaveraged vi(t) waveform is properly triggered (stationary). You may have to adjust the "trigger level" knob on the right-hand side of the oscilloscope panel. Then hit the "***Acquire***" button, and then press the "***Averaging***" soft key located under the scope display. Next, hit the ***"# Avgs***" soft key, and select "***64***" with the selector knob located to the right of the scope display. Now the vin(t) waveform should now look much less fuzzy!

   Once the oscilloscope is in averaging mode, the "***Quick Measure***" feature of the oscilloscope can be used to read the peak-to-peak value of vin(t) reliably. You will find that the peak-to-peak value of vin(t) displayed on the oscilloscope is a little bit less than the peak-to-peak voltage displayed on the function generator. This is due to the fact that the function generator is "loaded" by the input resistance of the amplifier due to the internal Rs = 50 ohm resistance of the function generator, as shown inside the dotted box in Fig. L6-1. Some of the available function generator voltage (as displayed on the function generator) is lost across the internal resistance of the meter. Make a slight upward adjustment in the function generator output voltage amplitude, so that the peak-peak value of vin(t) as read on the scope corresponds to 10 mV peak-peak. By simultaneously displaying the peak-to-peak voltage both at the input terminals, vi(t), and at the output terminals, vo(t), you can take the ratio of these two readings to measure the voltage gain, Avt = vo(t) / vin(t) of this amplifier. (Hint: your observed value of Avt should be close to the value predicted in the prelab. If your observations deviate by more than + or – 25% from this value, see the instructor.)

Remember to hit the "***Normal***" soft key to exit the averaging mode when you are ready to go on to the next measurement. If you forget and keep the scope in averaging mode as you probe a new point in your circuit, your scope display will often be incorrect, since the new waveform may not be properly triggered. While in averaging mode, if the averaged periodic signal (which should be largely noise-free) begins to undulate slowly in amplitude, this is a sign that your signal has lost triggering. If this happens, you must exit the averaging mode by hitting the "***Normal***" soft key, and take steps to re-trigger the signal to make it stationary before re-entering the averaging mode.

Include a copy of the oscilloscope screen showing both vin(t) and vo(t) as **Exhibit D**. Make sure the scope capture shows the peak to peak magnitude of both waves and then calculate the observed transducer voltage gain, Avt = vo(t) / vin(t) directly below the waveform as part of the attachment.

Does vo(t) appear to be a perfectly undistorted (though inverted) sinusoid? Recall that our in-class amplifier analysis has assumed "small signal" deviations about a bias point. However, in this case, vo(t) should have an amplitude of about Avo*10 mV peak-peak, which may be on the order of 1 volt peak-peak. This is ***not*** such a small deviation from the Q-point. Some small degree of distortion might be expected. Compare your observed value of Avt with the value of Avt *predicted by your hand calculations* (calculate % error).

Repeat your gain measurements with the emitter bypassed capacitor C_E removed. For this case, you may increase the signal strength to 100 mV peak-peak, since the gain of the amplifier is much lower now. (Hint: your Avt value should be close to the value predicted in the prelab. If it is far from this value, see the instructor.) Include a scope capture of vin(t) and vo(t) with the emitter bypass capacitor removed as **Exhibit E**. Again make sure to show the peak to peak amplitudes of both waves and to calculate the gain based on the measured amplitudes directly on the attachment.

	CE Present		CE Removed
Observed Avt =	_____	Observed Avt =	_____
Predicted Avt =	_____	Predicted Avt =	_____
Percent Deviation =	_____	Percent Deviation =	_____

5) Now (with C_E placed back in the circuit) gradually increase the amplitude of your input *sinusoidal* source upward from 10 mV peak-peak. At some point, either the positive or the negative peak of the sinusoidal output waveform vo(t) should begin to distort (flatten). Increase the input level until both the positive and negative peaks of the waveform are *clearly flattened*. Include a scope capture of vin(t) and the distorted vo(t) as **Exhibit F1**. On this screem capture, display maximum and minimum vo(t) voltage excursions. The difference between Vmax and Vmin shall be called "***maximum asymmetrical output voltage swing***".

Then decrease the input amplitude until the point is reached where the output waveform has ***only one*** of its peaks beginning to clearly flatten. Include a scope capture of vin(t) and the (still somewhat) distorted vo(t) as **Exhibit F2**. On this screen capture, display maximum and minimum vo(t) voltage excursions. The difference between Vmax and Vmin shall be called "***maximum symmetrical output voltage swing***"

6) Sketch both the DC and the AC load lines for this circuit ***directly over*** the BJT's common-emitter "Ic vs. Vce" characteristics that you plotted in Part 1. Next, use the AC load line, as explained in the section below (***Review of Maximum Symmetrical Voltage Swing Calculation***") to

approximately predict the maximum asymmetrical and symmetrical vo(t) waveform swing. Note that positive vo(t) peak flattening corresponds to driving the BJT into cutoff, while negative peak flattening corresponds to driving the BJT into saturation. Note that the vo(t) waveform is the vce(t) waveform with its dc component removed by the output coupling capacitor.

Show your calculations in the space below, and fill in the blanks below that compare the observed maximum asymmetrical and symmetrical vo(t) swing with your predictions. Your predicted and observed distortion points should agree within + or – 20%.

Calculation of maximum asymmetrical and symmetrical vo(t) output voltage swing

Predicted and observed distorted maximum asymmetrical vo(t) swing

Vo(t) max asymm swing (predicted) = _____ V peak-to-peak

Vc(t)max asymm swing (observed) = _____ V peak-to-peak

% deviation = _____

Predicted and observed distorted maximum symmetrical vo(t) swing

Vo(t) max symm swing (predicted) = _____ V peak-to-peak

Vc(t)max symm swing (observed) = _____ V peak-to-peak

% deviation = _____

Review of Maximum Symmetrical Vce(t) Swing Calculation

The "dc" bias load line is determined by writing KVL around the collector loop in the dc model of the circuit shown in Fig. L6-1. Assuming Ic is approximately equal to Ie yields:

$$Vcc = IcRc + Vce + Ic*Re + Vee \quad => \quad Ic = -Vce/(Rc + Re) + (Vcc-Vee)/(Rc + Re)$$

Note that Vcc = +12 V and Vee = -12 V. Thus the dc load line has an Ic axis intercept of (Vcc-Vee)/(Rc + Re) and a Vce axis intercept of (Vcc-Vee) = 24 V; it has a slope of -1/(Rc + Re); and it must intersect the BJT's Ic vs. Vce curve corresponding to $Ib = Ib_Q$ at the quiescent operating (Q) point.

The dynamic "ac" load line still passes through the Q-point, but it has a steeper slope than the dc load line. This is because in the ac model of the circuit of Fig. L6-1, the emitter resistor is short-circuited, and R_C is effectively connected in parallel with R_L. The slope of the dynamic (ac) load line is determined by applying KVL around the output loop in the ac model of the common emitter BJT amplifier, which reveals

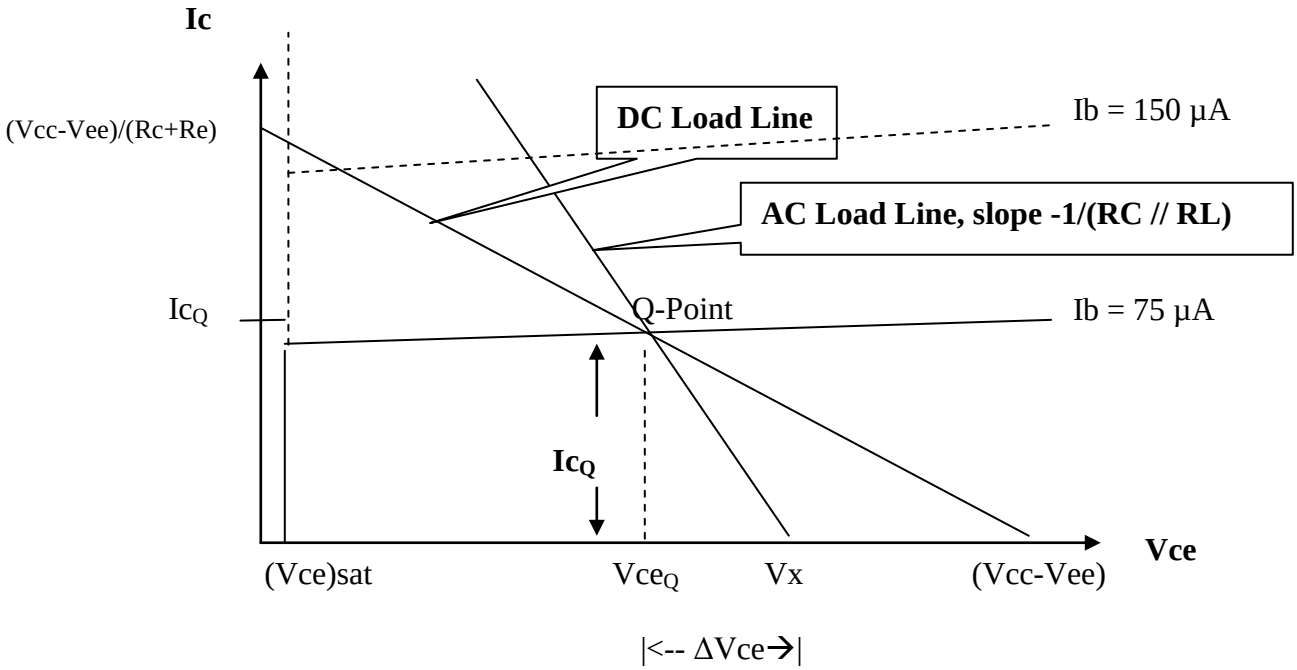
$$v_{CE}(t) = -(R_C \,//\, R_L)i_C(t)$$

Solving for $i_C(t)$:

$$ic(t) = -v_{CE}(t)/(Rc \,//\, R_L)$$

Thus the slope of the ac load line will be ***steeper*** than the slope of the dc load line, since the dc load line has a slope of $-1/(R_C + R_E)$, and the ac load line has a slope of $-1/(R_C \,//\, R_L)$. Note that when the complete Ic(t) and Vce(t) waveforms are considered (where the ac and dc parts of this problem are superimposed), this ac load line must still pass through the dc Q-point. The dc and ac load lines are plotted over the collector characteristics for a BJT in Fig. L6-3. Note that with the much steeper slope, even relatively small ac output voltage variations (resulting in excursions from V_{CEQ} of just a few volts) can cause the BJT to enter cutoff, thus resulting in a clipping-type of distortion as the sinusoidal source amplitude is increased, causing the amplitude of $vo(t) = v_{CE}(t)$ to rise to the point where the BJT enters cutoff on the high end, and saturation on the low end of the AC load line.

Fig. L6-3 Example BJT Collector Characteristic with dc and ac lines for CE amplifier



Thus to find the maximum symmetrical swing, we know the slope of the AC load line may be calculated two different ways:

$$\text{Slope AC Load Line} = -1/(Rc \,//\, RL) = -I_{CQ} / \Delta Vce$$

We may solve for ΔVce, which is the amount that Vce may rise above the Q-point value (Vce_Q) before the BJT leaves the active (amplifying) region and enters cutoff. Also, we must calculate the amount Vce may fall below Vce_Q before it leaves the active region and enters saturation, which is given by (Vce_Q – (Vce)sat). Since we usually want to know the maximum ***symmetrical*** swing of the output voltage Vce(t) about the Q-point, we take the ***smaller*** of these two calculated voltage swings as setting the maximum symmetrical swing.

For the drawing above, it is clear that ($Vx - Vce_Q$) < (Vce_Q – (Vce)sat), so the maximum symmetrical swing is given by

Max Symmetrical Output Voltage Swing = $2(Vx - Vce_Q) = 2\Delta Vce$ *(Volts, peak-to-peak)*

The highest possible value of Vce is:

$$(Vce)max = Vx = Vce_Q + \Delta Vce$$

The lowest possible value of Vce is:

$$(Vce)min = (Vce)sat.$$

=> ***Max Asymmetrical Output Voltage Swing*** = (Vce)max – (Vce)min

= Vx – (Vce)sat *(Volts, peak-to-peak)*

Appendix A. ECE250 Using the Sony-Tektronix 370 Curve Tracer To Trace Common-Emitter Ic vs. Vce curves of an NPN BJT

1. Depress **POWER** on/off button to turn on the power to the cuve tracer, if necessary. (This button is located at the extreme lower right of the panel).

2. Depress the "**STANDBY**" device selector button located at the lower left of the panel. This disconnects both devices from the curve tracer until it is properly set up.

3. Gently tilt up the plastic electrical safety interlock protection shield, and insert a BJT in the lower right and/or in the lower left BJT socket. For the 2N2222A, with the flat side facing toward you, the pins come out the bottom in C B E order.

4. Close the plastic shield, as the curve tracer will NOT operate unless this safety interlock shield is closed, as a safety precaution.

5. Adjust the "**VERTICAL Current/Div**" selector knob (upper middle of panel) to "**5 mA/div**". This value is displayed at the upper right of the oscilloscope display (See Fig. 3-26). If this value is not visible, try advancing the "**Readout/Cursor Intensity**" knob located to the right of the oscilloscope display. (Once the curve has been displayed, this setting may be adjusted as desired.)

6. Adjust the "**HORIZONTAL Volts/Div**" selector knob if the number to **2V/div**. . (Once the curve has been displayed, this setting may be adjusted as desired.)

7. Turn the "**STEP/OFFSET Amplitude**" selector knob clockwise to **50 μA**. This makes the current step generator (See Figure 3-25) generate base current (Ib) current steps with a current increment between adjacent steps of $\Delta Ib = 50\ \mu A$. (The "+" current polarity should be selected for an NPN BJT, if not depress the **INVERT** button to select it.) . (Once the curve has been displayed, this setting may be adjusted as desired.)

8. Set the "**Collector Supply Max Peak Power Watts**" selector paddle switch to **0.4 W** (this paddle is located on the lower right panel). (This permits more of the curves to be displayed in the high current, high voltage region of the Ic vs. Vce plot.)

9. Finally, hit the "**LEFT**" or the "**RIGHT**" device select button (located at the lower left of the panel) to display the "Ic vs. Vce" family of curves(one curve for Ib = 0, one for Ib = 50 μA, one for Ib =100 μA, one for Ib = 150 μA, etc.) for either the BJT in the left or the right socket, as selected.

10. At this point, a white dot should appear at the lower left of the oscilloscope display screen. If not, try turning up the top-most intensity knob located to the right of the oscilloscope display. Advance the large "**VARIABLE**" knob located at the far lower right of the panel, in order to display the family of common-emitter BJT curves, as depicted in Fig. 3-26.

11. You may want to make further adjustments in the **VERTICAL Current/Div** knob, the **HORIZONTAL Volts/Div** knob, the **STEP/OFFSET Amplitude** knob, and the "**NUMBER OF STEPS**" selector paddle to suit your taste.

12. Note that β can now be read as $\Delta Ic/\Delta Ib$ from the oscilloscope display of the family of Ic vs. Vce curves, where ΔIc is the vertical distance between adjacent curves in the vicinity of the desired Q-point, and ΔIb is the current increment step that was chosen back in Step 7 (in our example, $\Delta Ib = 50\ \mu A$). Note that β can be read even more conveniently by using the "**β/div** = 100" number that is automatically displayed for us by the curve tracer, as seen in Fig. 3-26. The curve tracer saves us the inconvenience of having to any calculation by making the following calculation for us:

$$\textbf{β/div} = \Delta Ic/\Delta Ib = (5\ mA/div)/50\ \mu A = 100.$$

13. You can compare two BJTs easily by alternately depressing the "LEFT" and "RIGHT" device selector buttons. This permits two BJTs to be selected that have nearly the same characteristics, as is sometimes required in a circuit.

Appendix B.
Basic Operation of Curve Tracer --- From Tektronix Curve Tracer Manual)

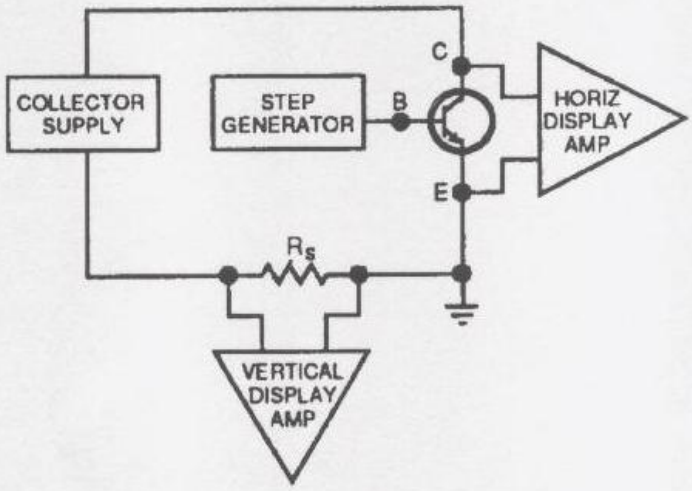


Figure 3–25: Bipolar Transistor Common-emitter Config

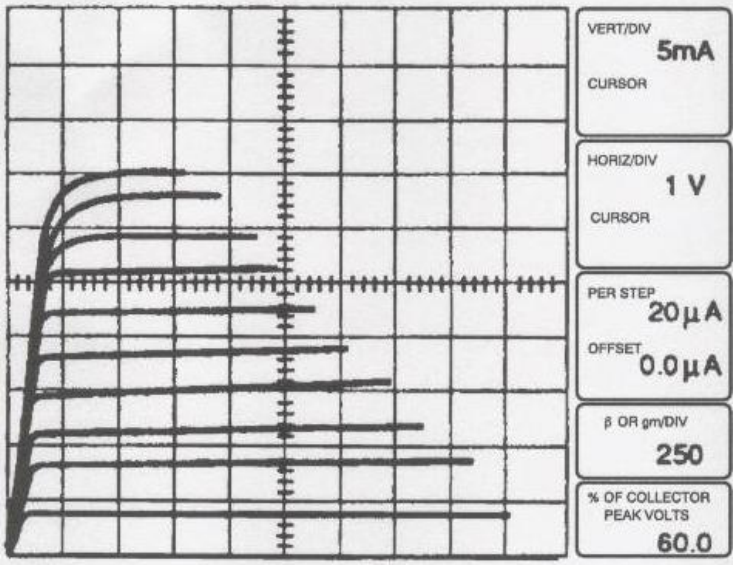


Figure 3–26: Bipolar Transistor Family of Curves