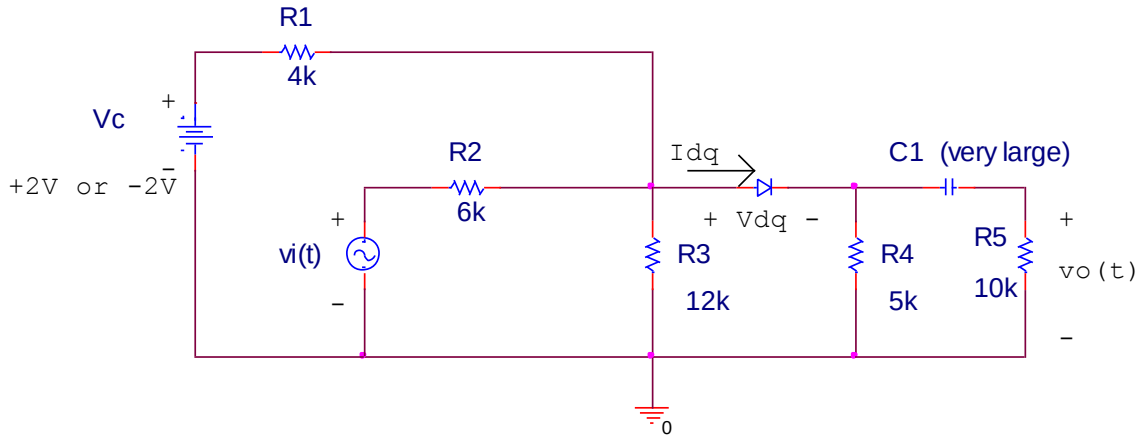
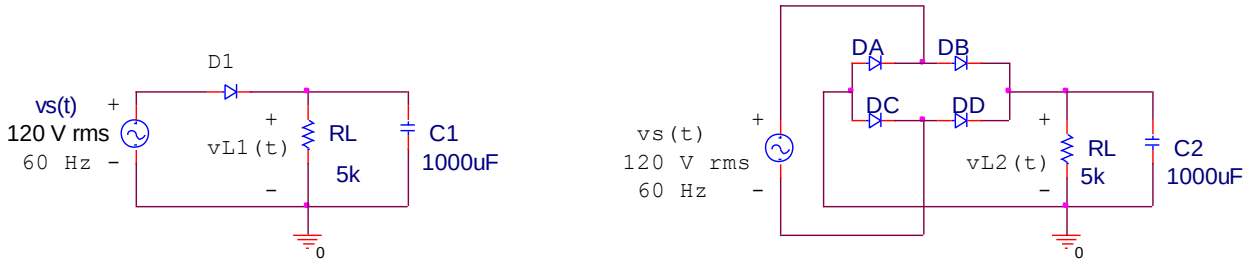
ECE250 Homework Assignment #3

1. Consider the analog diode switching circuit shown below. Assume the diode has reverse-saturation current Is = 10^{-10} A, emission coefficient n = 2, and internal (bulk) resistance rb = 0, and thermal voltage Vt = kT/q = 26 mV.



   a. Working as outlined in the course notes, draw the DC model of this circuit, and use Thevenin reduction to reduce the dc model to a single loop. Assume Vc = +2 V. Use the ideal diode equation to find the quiescent diode voltage and current, VdQ and IdQ. (Answer: 0.678 V, 46.06 μA)
   b. Calculate the diode's "ac resistance", rd. (Answer: 1129 Ω)
   c. Draw the ac model of the circuit. Use Thevenin reduction to reduce to a single loop. Calculate the ac (small signal) voltage gain of the circuit, Av = vo(t) / vi(t) when Vc = +2 V. (Answer: 0.172)
   d. What is the ac voltage gain of the circuit when Vc = -2 V? Explain.

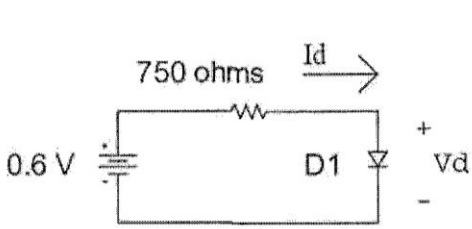
2. Consider the half-wave diode rectifier and the full-wave diode rectifier circuits shown below.

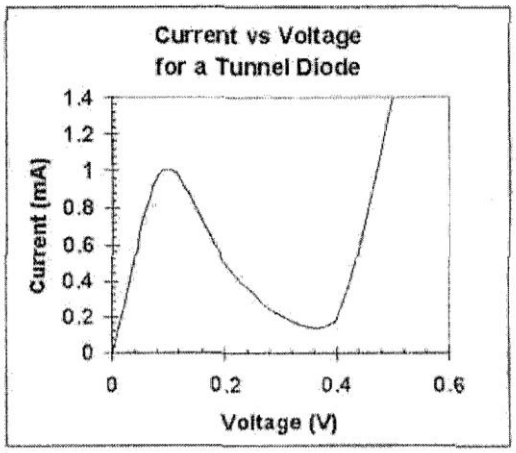


   a. Assume that all diodes have a forward voltage drop of 0.7 V. Find the peak-to-peak voltage variation of vL1(t), which is often called the "ripple voltage" Vr1. Also find the peak-to-peak voltage variation of vL2(t), which is often called the "ripple voltage" Vr2. (Answers: 0.562 V, 0.280 V --- your answers may vary be a few percent, depending upon the method you used.)
   b. What value of C is needed to reduce the ripple voltage to 0.20 V in each circuit above? (Answers: 2815 μF, 1402 μF --- your answers may vary be a few percent, depending upon the method you used.)
   c. What is the ripple voltage frequency for each of the circuits above? Briefly explain your reasoning. (Answers: 60 Hz, 120 Hz)
   d. What peak reverse voltage must be withstood by diode D1? (This is called the PIV rating of the diode.) By diode DB? (Answers: 338.7 V, 169 V)

3. Carefully trace the tunnel diode's nonlinear I-V curve onto your homework paper, and then draw a load line over this curve.

Use the graphical "load line" technique to find all possible solutions for Vd in the circuit below for the tunnel diode whose I-V curve is shown below with "Id" on the vertical and Vd on the horizontal axis. Note that a tunnel diode is a very special form of diode that breaks down at lower voltages due to a quantum mechanical tunnelling effect.



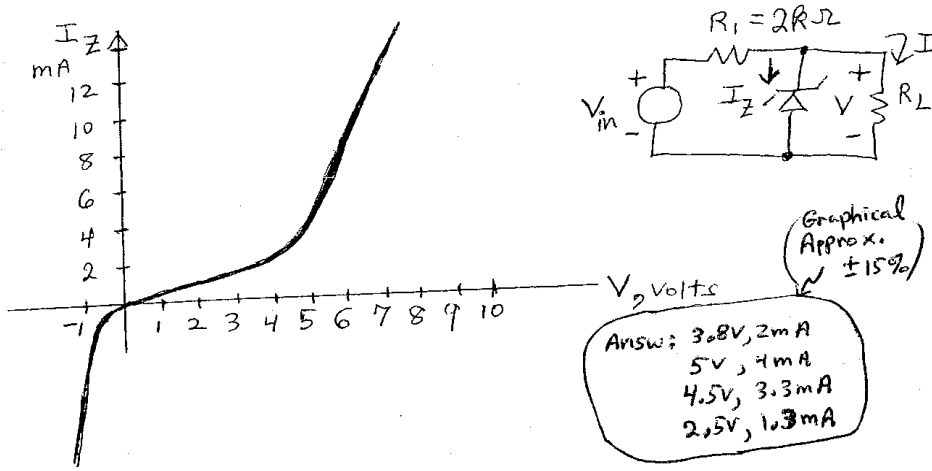


Vd = _____, _____, _____

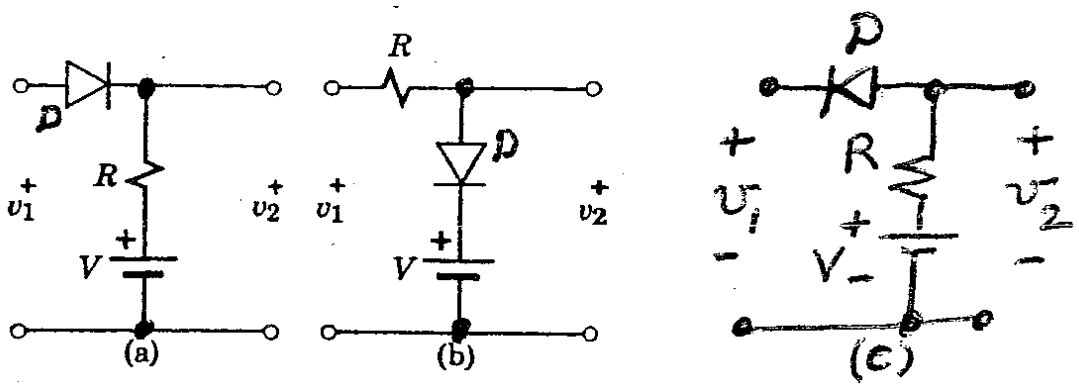
(Answ. ≈ 0.06V, 0.2V, 0.42V)

4. Carefully trace the Zener diode I-V curve shown below onto your homework paper, and draw the load lines for the voltage regulator circuit that is also shown below for each of the 4 cases indicated below. Then graphically determine the diode current (Iz) and the diode voltage (V) for each case. For which of these cases is the voltage regulator circuit pulled "farthest out of regulation"?

A. RL = 4 kΩ Vin = 10 V
B. RL = 4 kΩ Vin = 15 V
C. RL = 2 kΩ Vin = 15 V
D. RL = 1 kΩ Vin = 10 V

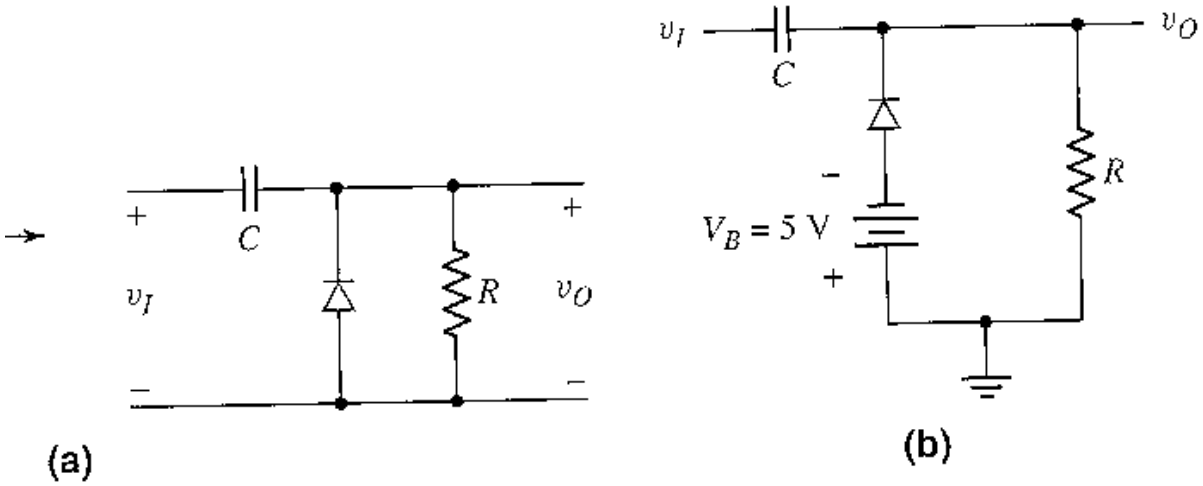


5. For v1(t) = 10sin(t) V., R = 1 kΩ, and V = 4 V., (A) sketch v2(t) for each of the circuits below. (B) Draw the voltage transfer curve (VTC) corresponding to each of the circuits below (v2 vs. v1) Assume the piecewise-linear diode model with Vγ = 0.7 V and Rb = 0 Ω. Let -10 V < v1 < 10 V in your VTC plots.



Partial answers for Part (B):
Circuit (a) : While v1 < 4.7 V => v2 = 4 V (D off); while v1 > 4.7 V, v2 = v1 – 0.7 V (D on)
Circuit (b): While v1 < 4.7 V, v2 = v1 (D off); while v1 > 4.7 V, v2 = 4.7 V (D on)
Circuit (c): While v1 < 3.3 V, v2 = v1 + 0.7 V (D on); while v1 > 3.3 V, v2 = 4 V (D off)

6. A. For the two circuits shown below, find expressions for the ***steady-state*** output voltage, vo(t), if each of the diodes has a forward voltage drop of Vγ = 0.7 V, and the source voltage is $v_I(t)$ = 10sin(t) V.



Because the RC time constant must be considerably greater than the source period (2π seconds), let C = 1000 μF and R = 1 MΩ.
(Answers: Circuit (a) vo = 10sin(t) + 9.3 V; Circuit (b) vo(t) = 10sin(t) + 4.3 V)

B. Now flip the diode around in each of the circuits shown above, keeping everything else the same. Repeat Part (A).
(Answers: Circuit (a) vo = 10sin(t) - 9.3 V; Circuit (b) vo(t) = 10sin(t) - 14.3 V)

7. Perform a PSPICE simulation of diode clamper Circuit (b) for both Part A and Part B of Problem 6. Use D1N4148 diodes (found in the PSPICE "EVAL" library) and VSIN sources in your simulation. *CAVEAT: Remember that in PSPICE, a component value of "1M" = 10^{-3}, and a resistor value of "1MEG" = 10^{6}!* For each of the two simulations, please include the PSPICE schematic diagram and also the corresponding PSPICE-generated "PROBE" plot of vo(t) and vi(t) on the same set of axes for each of these circuits. Show 3 – 4 cycles of vo(t), since it takes a while for the output to reach steady state. Be sure to mark and label the steady-state maximum and minimum values on these plots, using the "*cursor*", "*max*", "*min*", and "*mark*" icon buttons that appear at the top of the PROBE plot screen toolbar in PSPICE. Comment on the degree of similarity between these simulations and the predicted results from Problem 6 (the simulated results should match quite closely!)