GIVEN ~~74HC~~ 74VHC devices can operate with a 3.3V supply

FIND Power savings compared to 5 volt operation

SOLN

$P_{dynamic} \propto V_{cc}^2$

5V supply $\Rightarrow$ $V_{cc}^2 = 25\ V^2$

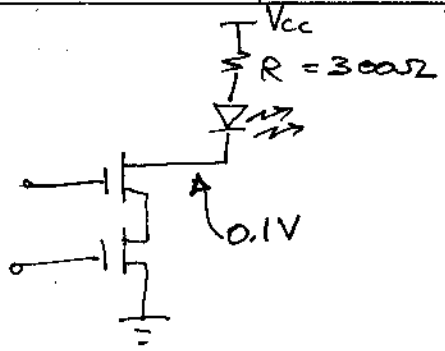
3.3 V supply $\Rightarrow$ $V_{cc}^2 = (3.3V)^2 = 10.9\ V^2$ } key results

$\Rightarrow$ $\frac{10.9 - 25}{25} \times 100\% = -56\%$

$\Rightarrow$ power is reduced a little more than a factor of two, ~~for~~ a drop by 56%

(there are multiple ways to compare the two numbers!)

GIVEN LED driven circuit :



FIND:

(a) current flowing through LED

(b) how much power is dissipated by the pullup resistor

SOLN

* Assume that LED forward bias voltage is 1.6V (see p.130 of text), & that Vcc is 5.0V (also see p.130)

⇒ voltage across resistor is $5 - (1.6 + 0.1) = 5 - 1.7$
$= 3.3\ V$

⇒ current through resistor is $\frac{3.3}{300} = \boxed{11\,mA}$ (a)
(& also through LED)

(b) Power dissipated by resistor is (current)^2(resistance)
or $\frac{(\text{voltage})^2}{\text{resistance}} = (11\,mA)^2(300) = \boxed{36.3\,mW}$ (b)

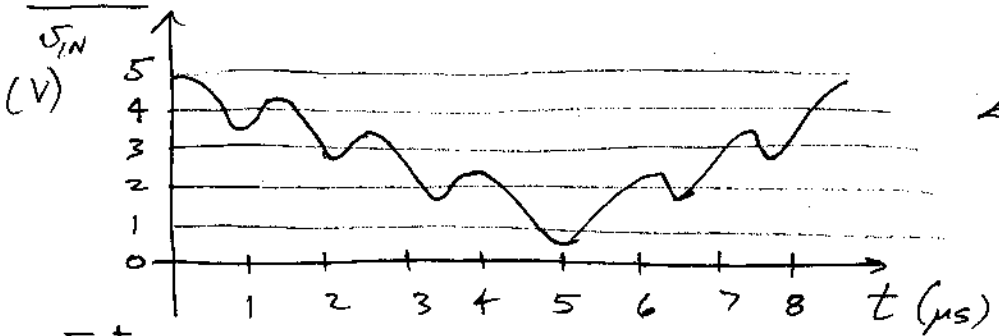
GIVEN Input waveform (see below)

FIND

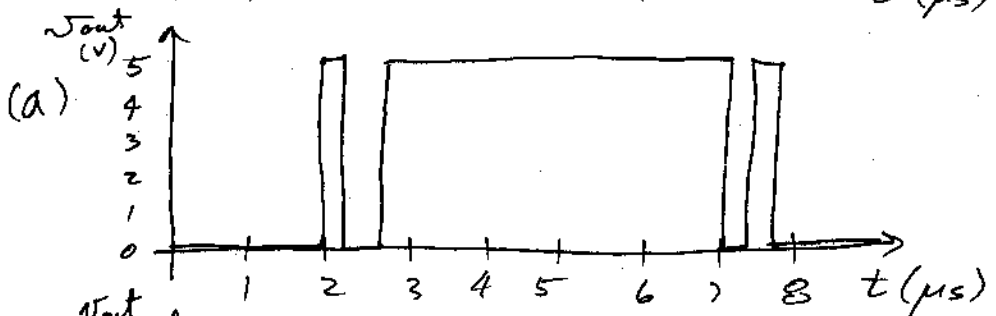
(a) Standard inverter response assuming 3.0V transition threshold

(b) Schmitt trigger inverter response (L to H threshold = 3.0V, H to L threshold = 2.0V)

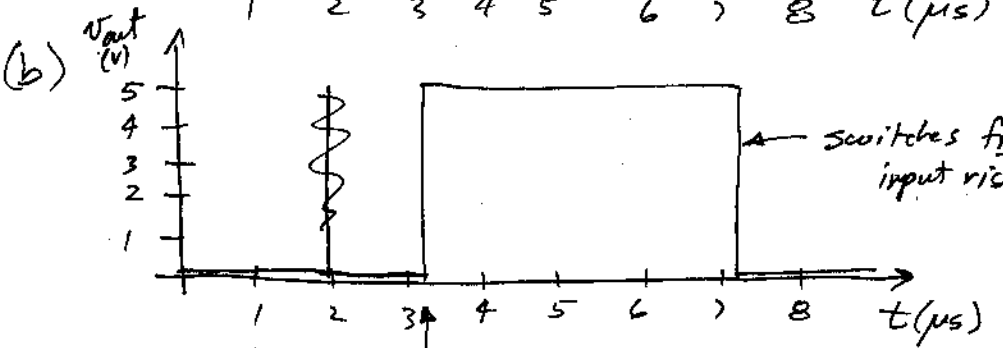
SOLN



← [approximate version of waveform on the HW sheet; times are not completely precise]



← [remember to make complete graphs... axis labels, scales, units]



← switches first time input rises above 3.0V.

switches first time waveform falls below 2.0V

TKOD 1

GIVEN (a) 7" of coaxial cable
(b) 3 yards of coaxial cable
(c) 5" of PCB tracing, outer surface

FIND Minimum permissible rise time to consider each system a "lumped" system

SOLN

* Assume the following propagation delays:

coax cable → 120 ps/in

FR4 PCB, outer trace → 140 ps/in (could also be as high as 180 ps/in)

* Need the t-line to be less than $l/6$ in length,

where $l = \frac{\text{rise time}}{\text{delay}}$

$$\Rightarrow \frac{t_r}{6 \cdot \text{delay}} < L \quad (L = \text{t-line length})$$

$$\text{or} \quad t_r > L \cdot 6 \cdot \text{delay}$$

(a) $t_r > (7")(6)(120\,ps/in) = 5.04 \times 10^3\,ps = \boxed{5.04\,ns}$

(b) $t_r > (3yd)\left(\frac{3\,ft}{yd}\right)\left(\frac{12\,in}{ft}\right)(6)(120\,ps/in) = \boxed{78\,ns}$

(c) $t_r > (5")(6)(140\,ps/in) = \boxed{4.2\,ns}$

GIVEN T-line Java applet

$Z_0 = 100\Omega$, look at voltage at end of line ($X = 100$)

Source termination methods:

(a) $Z_S = 20\Omega$, $Z_L = \infty$

(b) $Z_S = 20\Omega$, $Z_L = 20\Omega$

(c) $Z_S = 20\Omega$, $Z_L = 100\Omega$

(d) $Z_S = 100\Omega$, $Z_L = \infty$

(e) $Z_S = 100\Omega$, $Z_L = \infty // 100\Omega$

FIND - Evaluate each termination technique, specifically in terms of ① how quickly signal settles down, whether or not CMOS gate would get multiple transitions, & ③ whether or not the CMOS gate sees a solid HIGH level after transient has died out.

- Include waveform sketches.

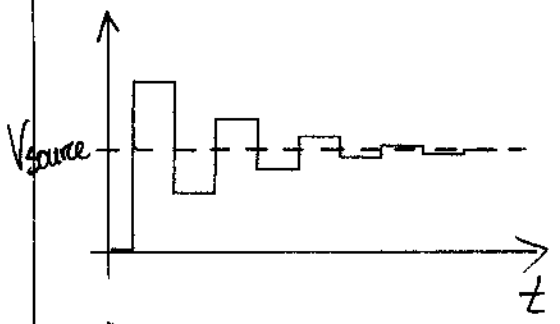
SOLN

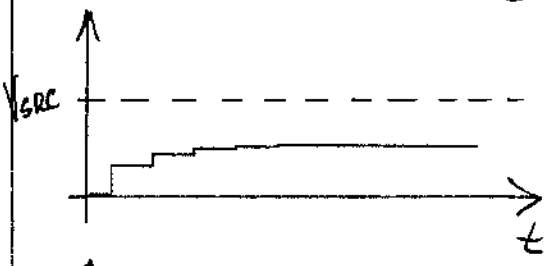
— See next page for plots & individual evaluations —

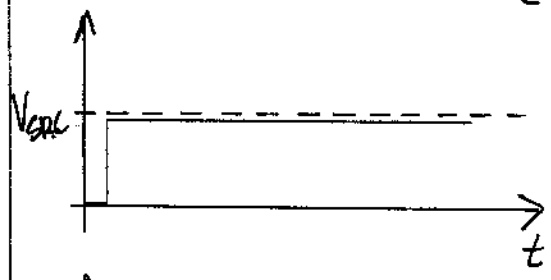
Overall best results obtained for cases (c) & (d).

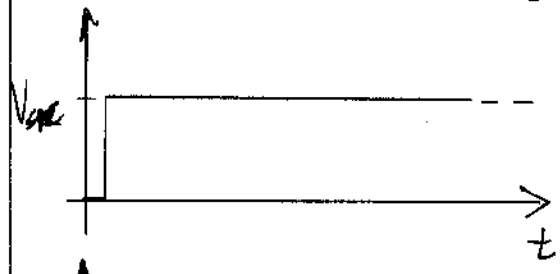
In both cases, only one end of the t-line is terminated by a matched load.

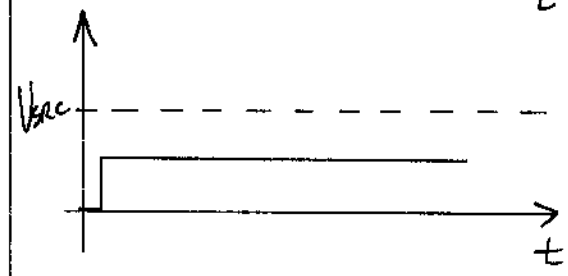
If termination resistance is the same as the source resistance, then the potential stabilizes to only half of the source voltage (voltage divider effect)











CRITERIA:

① Settling Time	② Multiple Transitions	③ Solid HIGH
LONG	MANY	YES
LONG	NONE	NO
FAST	NONE	YES (slightly low)
FAST	NONE	YES
FAST	NONE	NO

(a) Electro-Magnetic Compatibility

(b) See http://signalintegrity.com/Pubs/news/noEMC.htm

(c) Looking for a thoughtful response here!