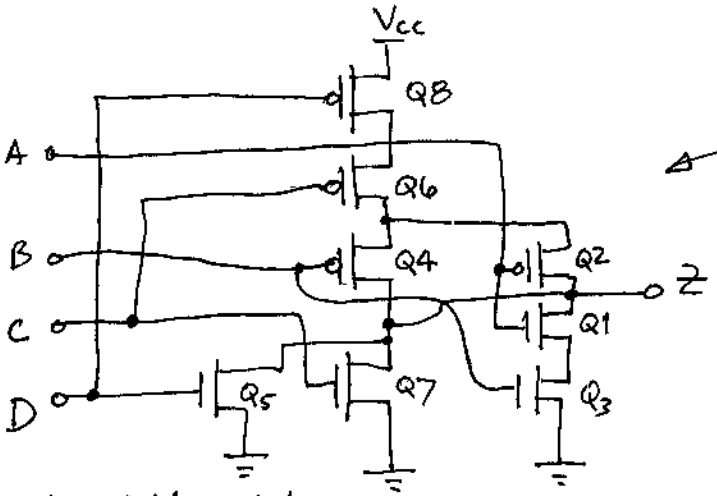
PROB 1

GIVEN



↑ A type of CMOS AND-OR-INVERT gate

FIND Function table & logic diagram using AND, OR gates & inverters

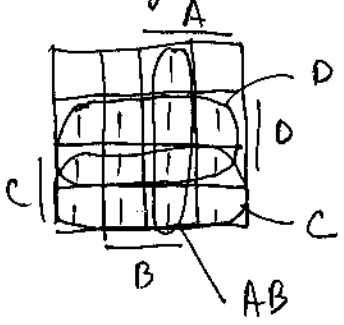
SOLN

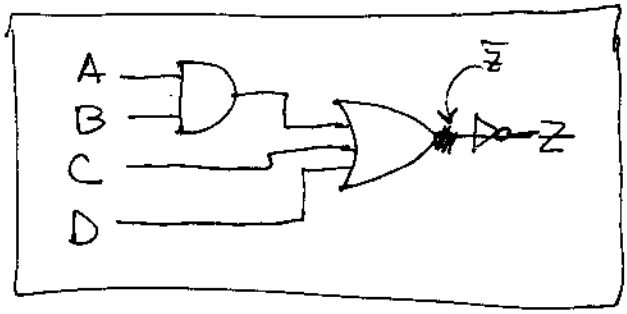
* Function table

(Transistor states ("-" = OFF, "1" = ON))

A B C D	Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	Z	
L L L L	- 1 - 1 - 1 - 1	H	← Q2, Q6 & Q8 ON ⇒ pull Z to Vcc
L L L H	- 1 - 1 1 1 - -	L	← Q5 ON pulls Z low
L L H L	- 1 - 1 - - 1 1	L	Q7 ON pulls Z low
L L H H	- 1 - 1 1 - 1 -	L	
L H L L	- 1 1 - - 1 - 1	H	← Q2, Q6 & Q8 ON ⇒ pull Z to Vcc
L H L H	- 1 1 - 1 1 - -	L	← Q5 ON pullz Z low
L H H L	- 1 1 - - - 1 1	L	Q7 ON pulls Z low
L H H H	- 1 1 - 1 - 1 -	L	
H L L L	1 - - 1 - 1 - 1	H	← Q4, Q6 & Q8 ON pullz Z high
H L L H	1 - - 1 1 1 - -	L	
H L H L	1 - - 1 - - 1 1	L	Q7 ON pullz Z low
H L H H	1 - - 1 1 - 1 -	L	
H H L L	1 - 1 - - 1 - 1	L	Q1 & Q3 ON ⇒ pull Z to ground
H H L H	1 - 1 - 1 1 - -	L	
H H H L	1 - 1 - - - 1 1	L	
H H H H	1 - 1 - 1 - 1 -	L	

* Logic diagram : plot K-map for $\bar{Z}$ (since looking for inversion at last part)



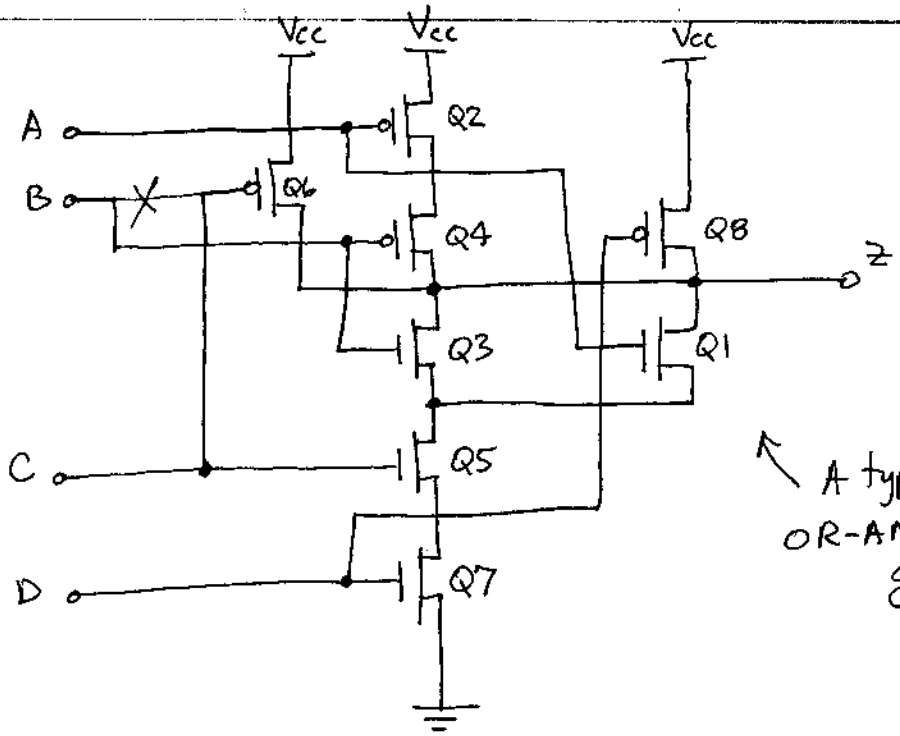


$\bar{Z} = AB + C + D$

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

PROB 2

GIVEN



↖ A type of CMOS OR-AND-INVERT gate

FIND Function table & logic diagram using AND, OR gates & inverters

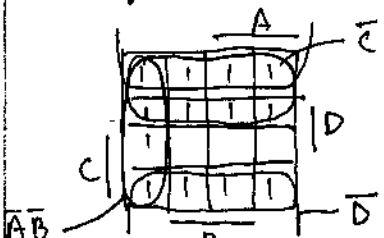
SOLN

* Function table

transistor states (" " = OFF, "•" = ON)

A B C D	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Z	
L L L L		•		•		•		•	H	← Q8 ON pulls Z high
L L L H		•		•		•	•		H	← Q6 ON pullz Z high
L L H L		•		•	•	X		•	H	
L L H H		•		•	•	X	•		H	← Q2, Q4 ON pull Z high
L H L L		•	•			•		•	H	
L H L H		•	•			•	•		H	
L H H L		•	•		•			•	H	
L H H H		•	•		•		•		L	← Q3, Q5, Q7 ON pull Z low
H L L L	•			•		•		•	H	
H L L H	•			•		•	•		H	
H L H L	•			•	•			•	H	
H L H H	•			•	•		•		L	← Q1, Q5, Q7 ON pull Z low
H H L L	•		•			•		•	H	
H H L H	•		•			•	•		H	
H H H L	•		•		•			•	H	
H H H H	•		•		•		•		L	

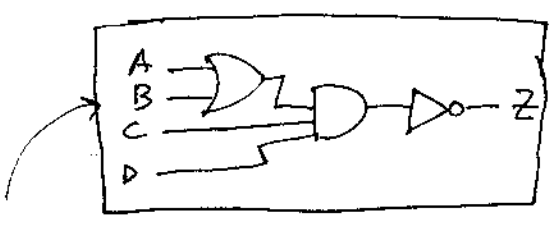
* Logic diagram : Plot K-map of Z :



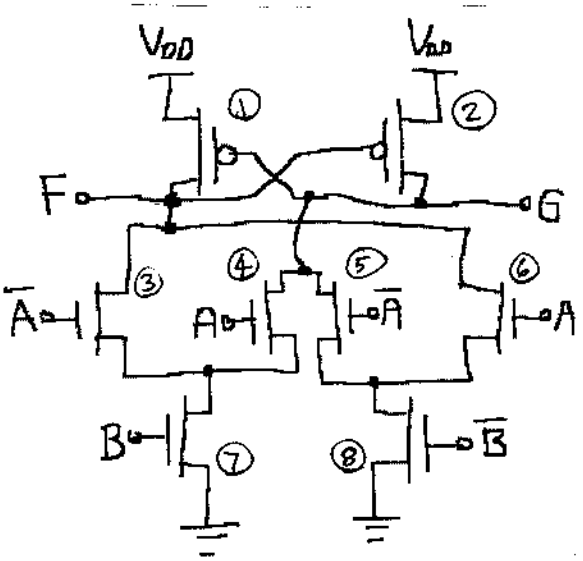
$Z = \bar{A}\bar{B} + \bar{C} + \bar{D}$

$\bar{Z} = \overline{\bar{A}\bar{B} + \bar{C} + \bar{D}}$

$= (A+B)(C)(D)$



GIVEN



FIND

(a) F & G as a function of A & B (use function table)

(b) Draw the circuit symbol of the gate

SOLN

(a) * Number the transistors as shown above

* Function table:

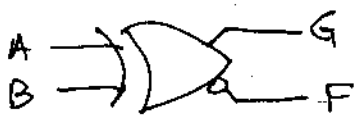
Inputs A	Inputs B	①	②	③	④	⑤	⑥	⑦	⑧	Outputs F	Outputs G	
L	L	ON	OFF	ON ~~OFF~~	OFF	ON	OFF	OFF	ON	H	L	← ⑤ & ⑧ ON pulls G low
L	H	OFF	ON	ON ~~OFF~~	OFF	ON	OFF	ON	OFF	L	H	← ③ & ⑦ ON pulls F low
H	L	OFF	ON	OFF ~~ON~~	ON	OFF	ON	OFF	ON	L	H	← ⑥ & ⑧ ON pulls F low
H	H	ON	OFF	OFF ~~ON~~	ON	OFF	ON	ON	OFF	H	L	← ④ & ⑦ ON pulls G low

G low pulls F high

F low pulls G high

NOTE: Transistors ③ through ⑧ cause primary action on output, & secondary action on transistors ① & ②.

(b)



(combination of EXOR & EXNOR gate)

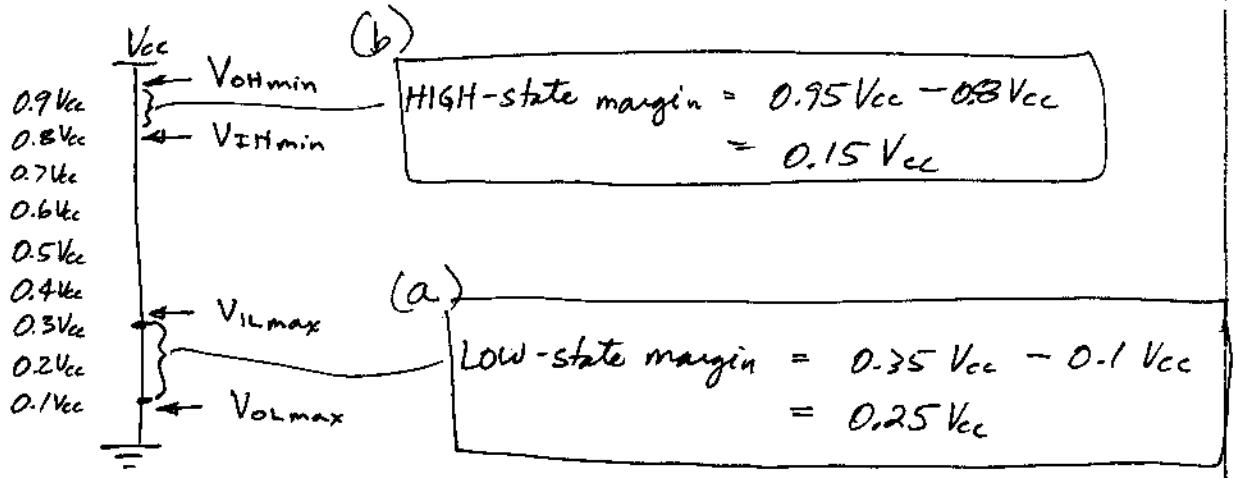
PROB 4

GIVEN Specifications for a particular logic family:

$V_{OL\,max}$ = ground + 10% of V_{CC}
$V_{IL\,max}$ = 35% of V_{CC}
$V_{IH\,min}$ = 80% of V_{CC}
$V_{OH\,min}$ = V_{CC} − 5% of V_{CC}

FIND
(a) LOW-state DC noise margin
(b) HIGH-state " " "
(c) Overall noise margin

SOLN



(c) Overall noise margin = minimum of HIGH-state & LOW-state margins = **0.15 V_{CC}**

HW2 Prob 5

GIVEN Data sheet of Wakerly Table 3-3

FIND Worst-case LOW-state & HIGH-state DC noise margins of the 74HC00. State any assumptions!

SOLN

* "Worst-case" implies that you use data sheet values that give pessimistic margins (i.e., low numbers) rather than optimistic margins (high numbers).

* Noise margins are defined as follows:

  LOW-state : $V_{ILmax} - V_{OLmax}$

  HIGH-state : $V_{OHmin} - V_{IHmin}$

* From Table 3-3:

  $V_{ILmax} = 1.35V$, $V_{IHmin} = 3.15V$

  $V_{OLmax} = 0.33V$ ← this is for max I_{OL} current of 4mA

  $V_{OHmin} = 3.84V$ ← this is for max I_{OH} of -4mA

* DC margins are then:

  LOW-state: $1.35 - 0.33 = 1.02V$

  HIGH-state: $3.84 - 3.15 = 0.69V$

PROB 6

GIVEN Three resistive loads:

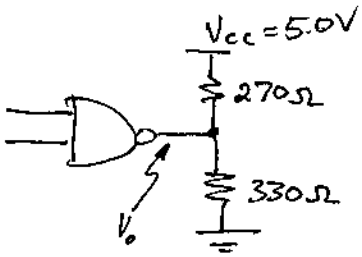
(b) $R = 330\Omega$ to GND & 270Ω to V_{CC}
(c) 100Ω to V_{CC}
(f) 75Ω to V_{CC} & 150Ω to GND

FIND Determine whether the output drive current specifications of the 74HC00 over the commercial operating range are exceeded. Use Table 3-3, $V_{OHmin} = 3.84V$ & $V_{CC} = 5.0V$.

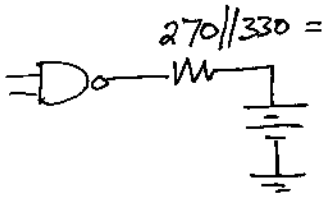
note corrected value from "Errata" sheet!!

SOLN

(b)



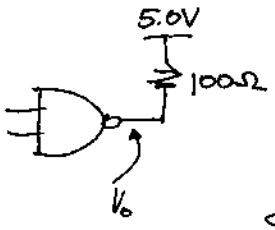
$\Rightarrow$



at $V_o = V_{OLmax} = 0.33V$ (from Table 3-3), the gate needs to sink $\frac{2.75 - 0.33}{149} = 16.2mA$ (this is greater than 4mA)

$\Rightarrow$ exceeds drive current

(c)

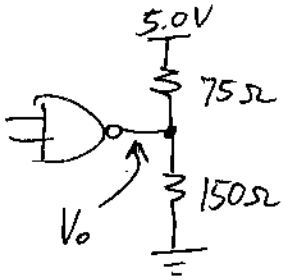


Worst case current is when output is LOW:

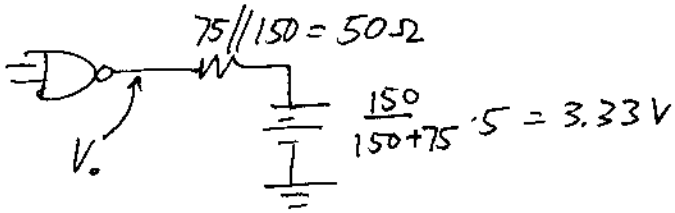
Sinking current is $\frac{5.0 - 0.33}{100} = 46.7mA$

exceeds drive current

(f)



$\Rightarrow$



worst case current is when output is LOW:

Sinking current is $\frac{3.33}{50} = \frac{5.0 - 0.33}{50} = 60mA$

$\Rightarrow$ exceeds drive current