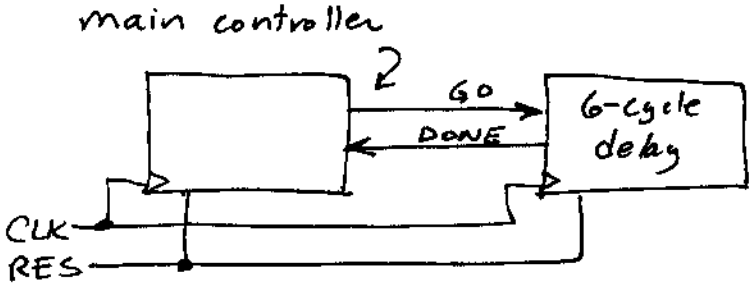
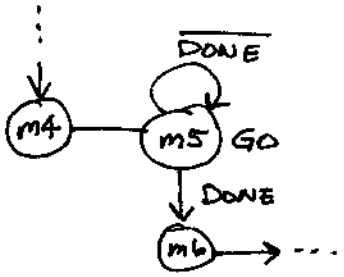
PROBLEM 1 : You are given the following information for a handshaking design:



"GO" & "DONE" are active high

Portion of main controller state transition diagram:



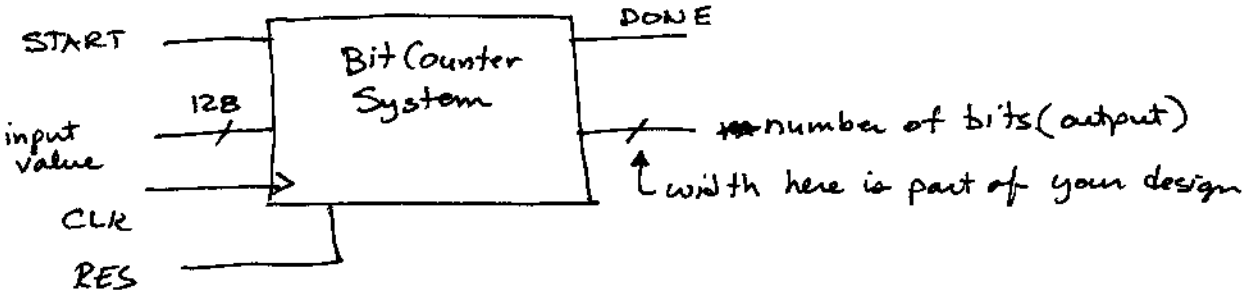
note that "GO" signal is generated in the same state as the wait for "DONE"

(a) Design the state transition diagram for the "6-cycle ~~dead~~ delay" device that will make the main controller stay in state "m5" for exactly six cycles.

(b) Draw the complete timing diagram that shows the handshaking signals as well as the states of the controller & 6-cycle delay.

PROBLEM 2 : Wakerly 8.20 (read 8.9.1 – 8.9.4)

PROBLEM 3: Design a data unit and controller for a system that counts the number of bits in a 128-bit input value that are logic "1":



- START is active high of duration one clock period
- DONE is normally high. DONE drops low while Bit Counter is processing the input, then goes high again when processing is complete.
- Present your Controller design as a state transition diagram
- Present a detailed block diagram of the data unit
- Clearly show all control signals from controller to data unit, and show all condition signals from data unit to controller.
- Data unit elements and controller FSM must all trigger on the rising edge of the clock input
- Write a paragraph that summarizes your overall approach to the design of this system