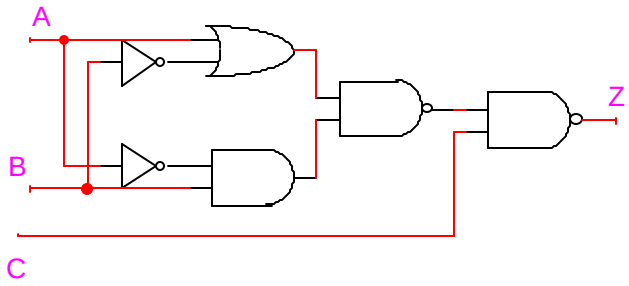
Name _____ Box _____ Due date: Tuesday. 5 Dec.

EC333 Homework #1 Winter 2000-2001

1 Find a simplified logic expression and fill in the truth table for the circuit below.



A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

2 Design minimal sum-of-products logic to produce Z=1 if at least two bits in ABCD are 1s. Present logic expression and draw gate level implementation.

ABCD	Z
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

CD \ AB	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	2	7	15	11
10	3	6	14	10

3 Design a controller with one 74LS193 4-bit counter and necessary gates for the 4-bit multiplier in Lab #1. Your controller should generate the following signals for the six select lines. See the attached data sheet for 74LS193.

(A) A master reset switch will start the controller.

(B) Ten states are generated in sequence as follows. The controller should hold the result after the sequence.

	Clock cycle									
Register	1	2	3	4	5	6	7	8	9	10
A	hold	Load	LS	Load	LS	Load	LS	Load	LS	Hold
B	Don't Care	Hold	LS	Hold	LS	Hold	LS	Hold	LS	Hold
C	Load	Hold	LS	Hold	LS	Hold	LS	Hold	LS	Hold

From a controller's point of view, the events can be set up as follows.

	S1 S0									
Register	1	2	3	4	5	6	7	8	9	10
A	00	11	10	11	10	11	10	11	10	00
B	XX	00	10	00	10	00	10	00	10	00
C	11	00	10	00	10	00	10	00	10	00

Hints: (1) Choose a natural sequence from the four outputs of the counter to represent the select signals.

(2) The optimum implementation may not need any gate other than inverters for the control lines.

(3) Extra logic is needed to hold the product after the 9^{th} clock pulse.