ECE130-02 Introduction to Logic Design

Spring Quarter 2001

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Office location: D209 Moench Hall

Class time and place: M, T, Th, F 9:55-10:45, G310 Crapo Hall
Textbook: Pragmatic Logic: A Non-idealistic, Practical, Opinionated Look at Digital Logic Design. William J. Eccles (RHIT publication)
Simulation software: LogicWorks-4 for Windows from Capilano Computing
Office Hours: MTR/6-7, W/2-3 (or just drop in)

Course Objectives

Fundamental concepts, analysis and design techniques of digital systems will be introduced through examples and simulation. Digital system design processes and methodologies will be learned and practiced with homework problems and a team project. Upon the completion of this course, the student should be able to analyze and design combinational and sequential circuits as well as to complete a digital system design project from conceptual development, sub-module designs, to system integration.

General Policies

Grading Policy:

Homework:	10%
In-class exercises & quizzes	5%
Three Tests:	45%
Project:	20%
Final Exam:	20%

Homework: Homework will be assigned daily. Unless otherwise noted, the homework will be due at the BEGINNING of the next class period. Late homework will be accepted with a grade reduction of 20% for each day that it is late.

Tests: Three full-class-period tests are scheduled on March 23, April 5 or 6, and May 4. The tests are closed book and closed notes.

Project: A design project will be performed in a team of a number of students. The project report will be due by 5:00 PM on Thursday, 17 May. Grading for the project will have the following breakdown.

Block Diagram Memo	5%
State Diagram Memo	10%
Verification Memo	15%
Simulation	15%
Final Written Report	35%
Oral Presentations	20%