

# Instruction Scheduling

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## Instruction Cycles

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Not all instructions are equal.

- Load/Store: 3 cycles
- Add: 1 cycle
- Multiply: 2 cycles

Multi-cycle instructions can be interleaved in the processor pipeline

## Examples with Cycles

| Start | Operations           |
|-------|----------------------|
| 1 3   | loadAI rarp,@a ⇒ r1  |
| 4 1   | add r1,r1 ⇒ r1       |
| 5 3   | loadAI rarp,@b ⇒ r2  |
| 8 2   | mult r1,r2 ⇒ r1      |
| 10 3  | loadAI rarp,@c ⇒ r2  |
| 13 2  | mult r1,r2 ⇒ r1      |
| 15 3  | loadAI rarp,@d ⇒ r2  |
| 18 2  | mult r1,r2 ⇒ r1      |
| 20 3  | storeAI r1 ⇒ rarp,@a |

22 (a) Original Code

| Start | Operations           |
|-------|----------------------|
| 1 1   | loadAI rarp,@a ⇒ r1  |
| 2 1   | loadAI rarp,@b ⇒ r2  |
| 3 1   | loadAI rarp,@c ⇒ r3  |
| 4 1   | add r1,r1 ⇒ r1       |
| 5 1   | mult r1,r2 ⇒ r1      |
| 6 1   | loadAI rarp,@d ⇒ r2  |
| 7 2   | mult r1,r3 ⇒ r1      |
| 9 2   | mult r1,r2 ⇒ r1      |
| 11 3  | storeAI r1 ⇒ rarp,@a |

13 (b) Scheduled Code

## Constructing a Dependence Graph

Start with the last instruction of a block of code.

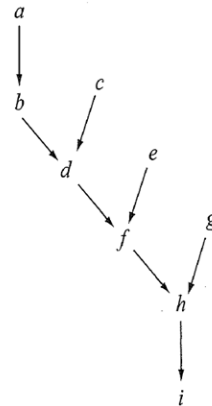
Work up, adding arrows indicating which instructions depend on which data.

## Dependence Graph (Finally a real tree!)

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a: loadAI  rarp,@a ⇒ r1
b: add     r1,r1 ⇒ r1
c: loadAI  rarp,@b ⇒ r2
d: mult    r1,r2 ⇒ r1
e: loadAI  rarp,@c ⇒ r3 r2
f: mult    r1,r2 ⇒ r1
g: loadAI  rarp,@d ⇒ r2
h: mult    r1,r2 ⇒ r1
i: storeAI r1      ⇒ rarp,@a
  
```

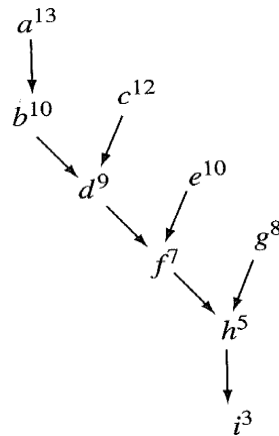
(a) Example Code



(b) Its Dependence Graph

## Annotated Dependence Graph

Next, add sums of latencies  
to the nodes of the graph:  
We will use this information  
later for inserting nodes into  
a (max) priority queue



## List Scheduling Algorithm

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A greedy algorithm.  
 Has been used since  
 Babbage (I swear!)  
 Ready is a priority  
 using the latency times  
 as a criteria for insert,

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Cycle ← 1
Ready ← leaves of  $\mathcal{D}$  // Max PriorityQueue
Active ←  $\emptyset$  // Queue
while (Ready  $\cup$  Active  $\neq \emptyset$ )
  for each  $op \in$  Active
    if  $S(op) + delay(op) \leq Cycle$  then
      remove  $op$  from Active
    for each successor  $s$  of  $op$  in  $\mathcal{D}$ 
      if  $s$  is ready
        then add  $s$  to Ready
  if Ready  $\neq \emptyset$  then
    op ← poll(Ready)
     $S(op) \leftarrow Cycle$ 
    add  $op$  to Active
  Cycle ← Cycle + 1
  
```