CSSE 332 -- OPERATING SYSTEMS

Multi-level Page Tables

Name: SOLUTION KEY

Question 1. (10 points) Based on our discussion of a two-level page table with 16-bits addresses and 16-bit PTEs, draw how the following address would be used to lookup the corresponding physical address: `0x3D0B`.

Make sure to show your offset inside each page. Assume that the address of the first level page table is already provided in the appropriate register.

Solution: Solution provided in class.

Question 2. (5 points) Describe the RISC-V organization of a 64-bit address to support multi-level page tables. Make sure to label each section of the address with its use in the address translation.

636261605958575655545352515049484746454443424140393837363534333231302928272625242322212019181716151413121110 9 8 7 6 5 4 3 2 1 0

Unused	Level 2 addr	Level 1 addr	Level 0 addr	Page offset

Question 3. (5 points) In RISC-V, the address of the first level page table for every running process is stored in the _____`satp`_____ register.

Question 4. Assume we are dealing with `4 KB` pages in RISC-V with the address breakdown from **Question 2**. Answer the following questions.

(a) (5 points) How many page table entries (PTEs) does each page of the page table contain?

Solution:

Each PTE address is 9 bits, which means we have$2^9 = 512\texttt{PTEs}$.

(b) (5 points) Given that, how wide if a PTE?

Solution: We have 4 KB pages with 512 PTEs per page. This means we have $\frac{2^2 \times 2^{10}}{2^9} = 2^3 = 8\texttt{bytes} = 64\texttt{bits}$.

(c) (5 points) Describe the breakdown of a PTE into its corresponding constituents.

Solution:

63 62 61 60 59 58 57 56 55 54	53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Unused	Frame Address	Flags